ULTRA-LOW-VOLTAGE IC DESIGN

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Outline

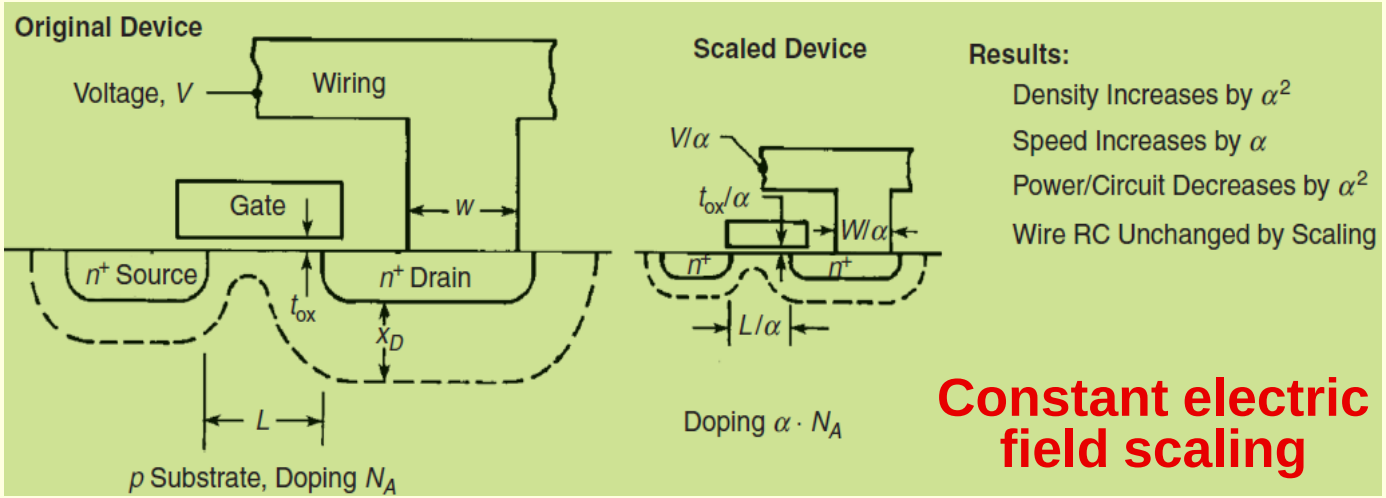
- 1 Introduction to ultra-low-voltage (ULV) CMOS
- 2 Subthreshold MOSFET model
- 3 Subthreshold CMOS logic and Schmitt trigger
- 4 ULV rectifiers
- 5 ULV oscillators

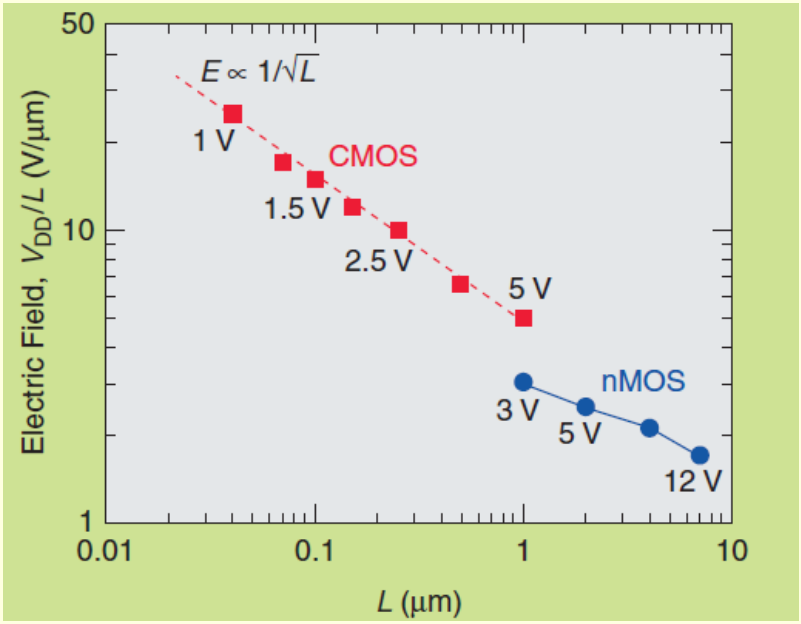
Chapter 1

Introduction to ultra-low-voltage CMOS

Motivations for low voltage

1. Scaling





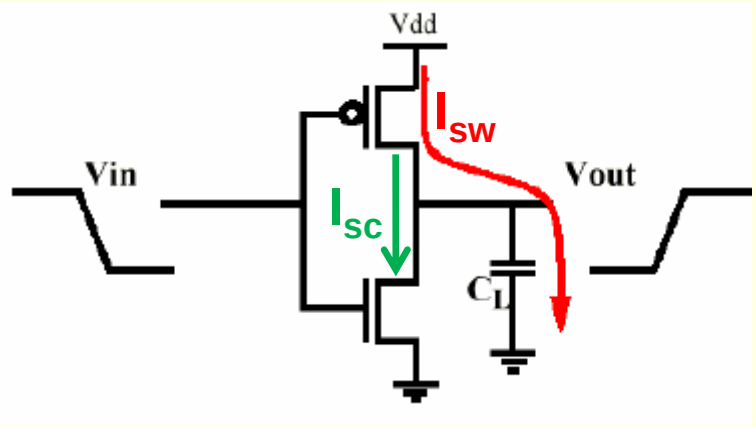
R. H. Dennard et et. al.
IEDM 72 & IEEE JSSC,
Oct. 1974

Motivations for low voltage

2. Power dissipation

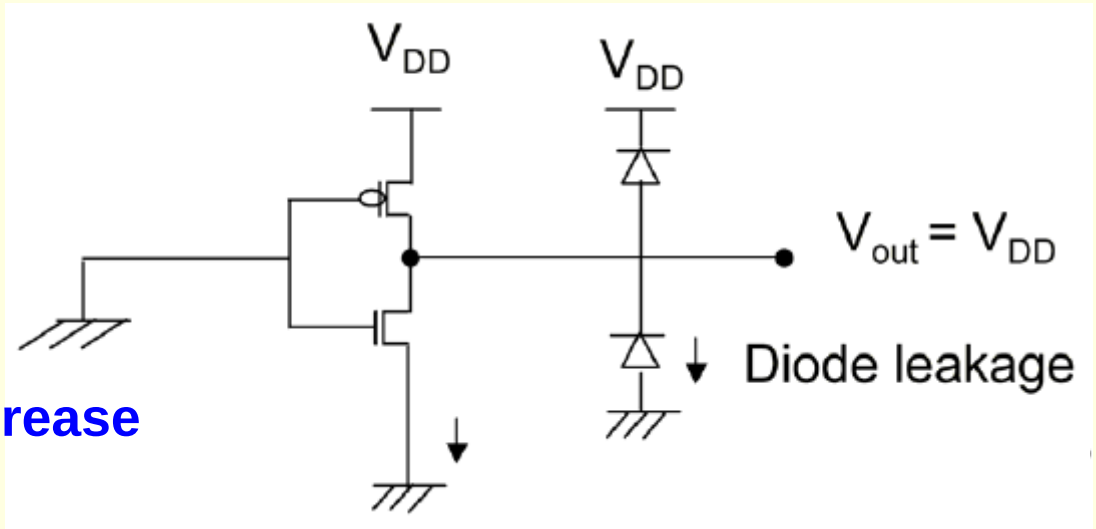
Switching power

$$\text{Power} = \text{Energy/transition} * f = C_L * V_{dd}^2$$



Short-circuit power :
due to non-zero rise/fall times

Leakage power α V_{DD}



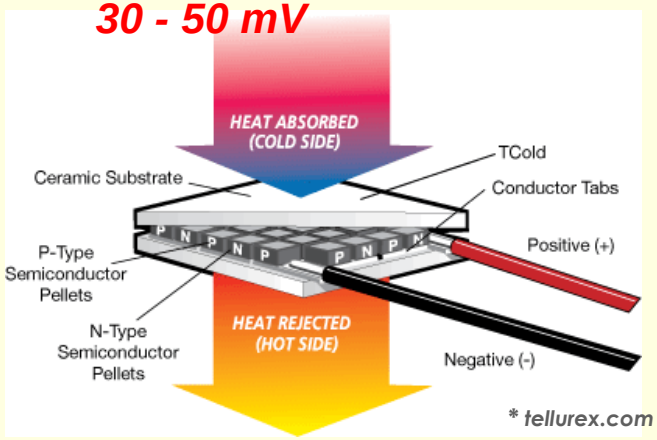
Most effective way to decrease power is to lower V_{DD}

Motivations for low voltage

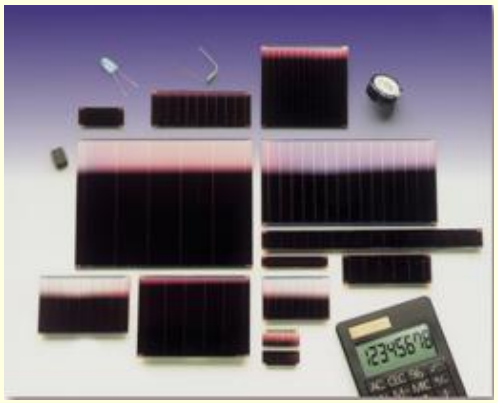
3. Low supply voltages

Thermoelectric generator

$V_{o(body\text{-}environment)} \approx$ *30 - 50 mV*



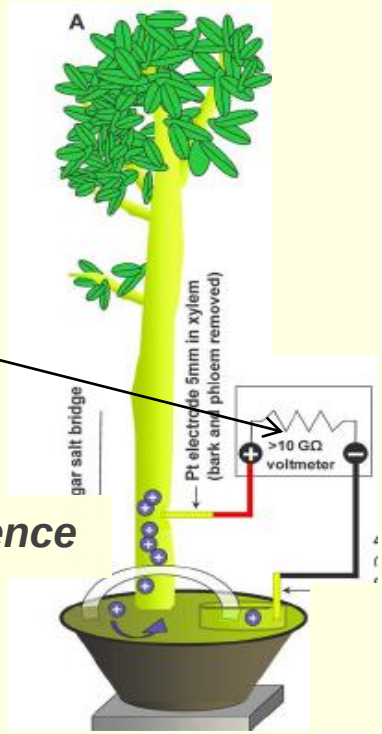
Photovoltaic cell



$V_{o(dark\ room)} \approx$ *100 - 200 mV*

Energy provided by trees

Vo ≈ 20-200 mV

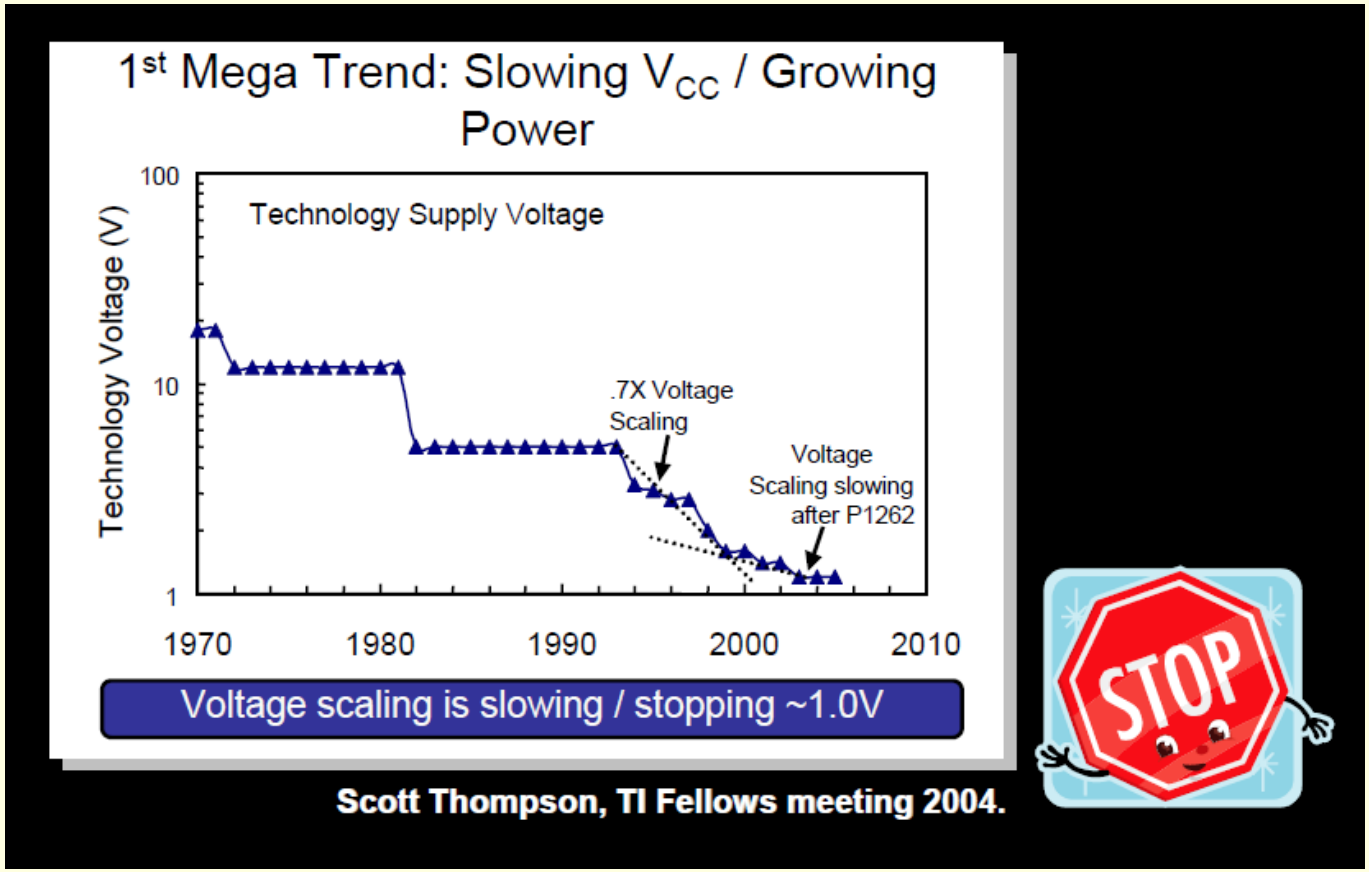


pH difference

** Love et al, "Source of sustained voltage difference between the xylem of a potted ficus benjamina tree and its soil", 2008.*

The trend toward low supply voltages

- Q1-Is there a lower bound for the supply voltage?
- Q2-What are the best technologies for ULV circuits?

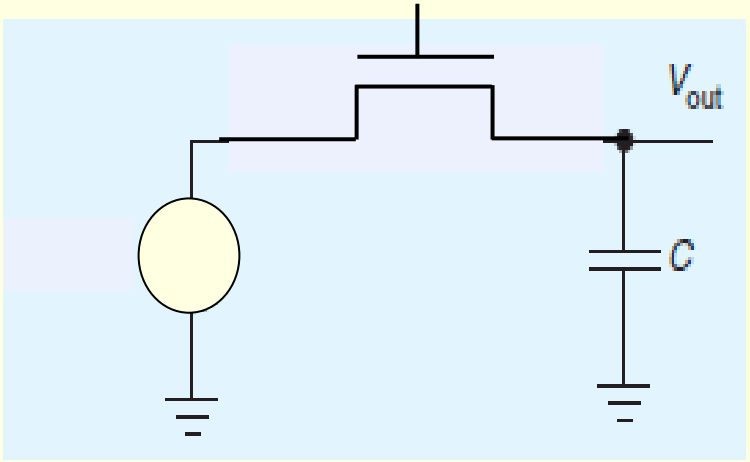


? ?

Fundamental limits on supply voltage

From thermodynamics

What is the minimum energy stored in a capacitor to ensure that the binary states are distinguishable in the presence of thermal noise?



Any energy storage element (or "degree of freedom") in thermal equilibrium holds an average noise energy of *kT/2.*

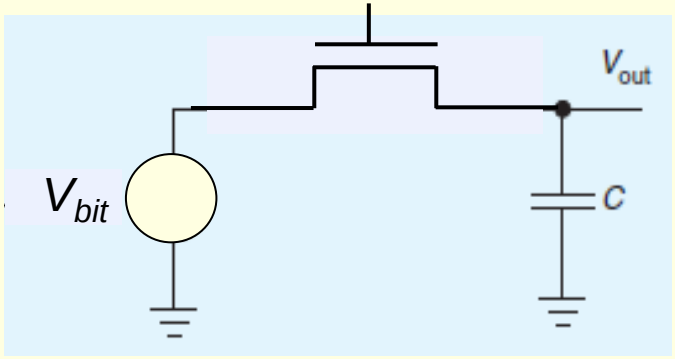
$$\overline{\frac{1}{2}Cv_{no}^2} = \frac{kT}{2}$$

$$\overline{v_{no}^2} = \frac{kT}{C}$$

Fundamental limits on supply voltage

From thermodynamics

What is the minimum energy stored in a capacitor to ensure that the binary states are distinguishable in the presence of thermal noise (Theis & Solomon 2010)?



The charge Q_{bit} stored in C is

$$Q_{bit} = CV_{bit} \Rightarrow V_{bit} > \frac{kT}{Q_{bit}} = \frac{kT}{Nq}$$

N is the number of electrons and q=1.6 x 10^{-19} C is the electron charge

The bit (=1) energy is $\frac{1}{2}CV_{bit}^2$

To distinguish bit energy from noise energy we must have

$$\frac{1}{2}CV_{bit}^2 > \frac{kT}{2} \Rightarrow V_{bit}^2 > \frac{kT}{C}$$

$$N = 1 \Rightarrow V_{bit} > \frac{kT}{q} = 25.9 \text{ mV}, C > 6.18 \text{ aF}$$

$$N = 1000 \Rightarrow V_{bit} > 25.9 \ \mu\text{V}, C > 6.18 \text{ pF}$$

Eight standard deviations give an error probability of ~ 10^{-15}

$$V_{bit} > 8\frac{kT}{Nq}$$

Thermal noise limits for supply voltages of logic and static memory

$V^2_{no} = kT/C$ (I)

Output node capacitance

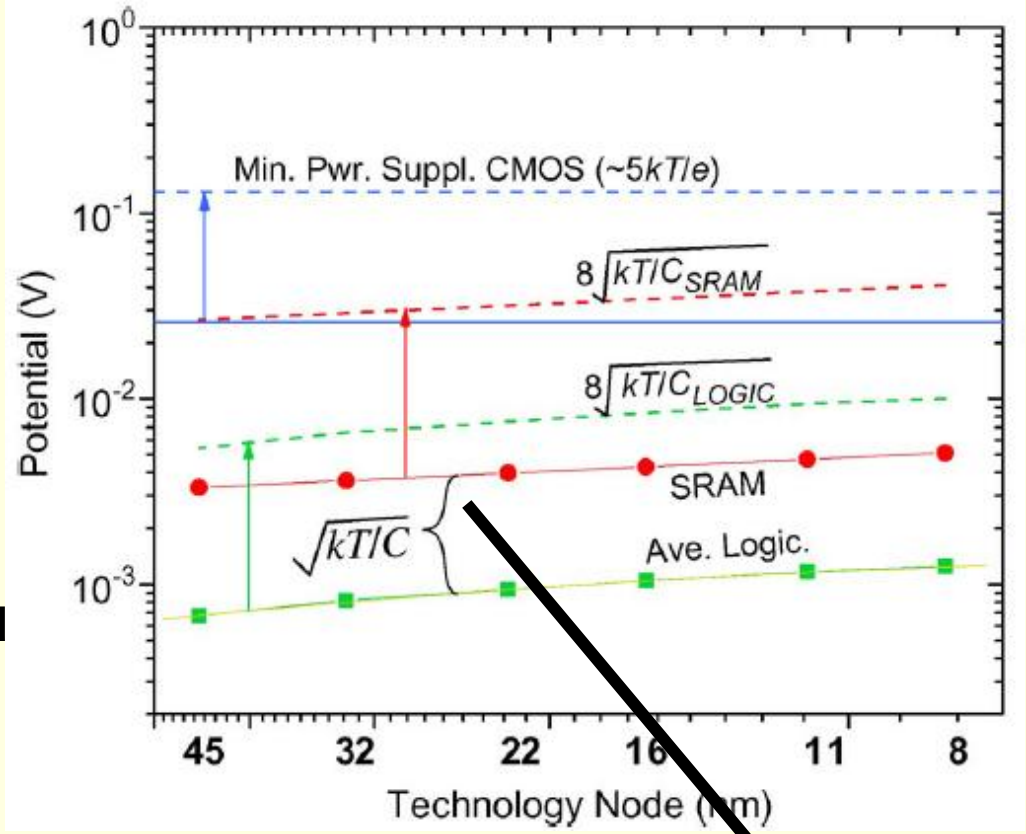
$V_{out} = Nq/C$ (II)

Number of electrons stored in the output node

For $V_{min} = V_{out} \sim V_{no}$

$V_{min} = V_{out} = (1/N)kT/q$

N =1 circuit storing a single electron in its output node

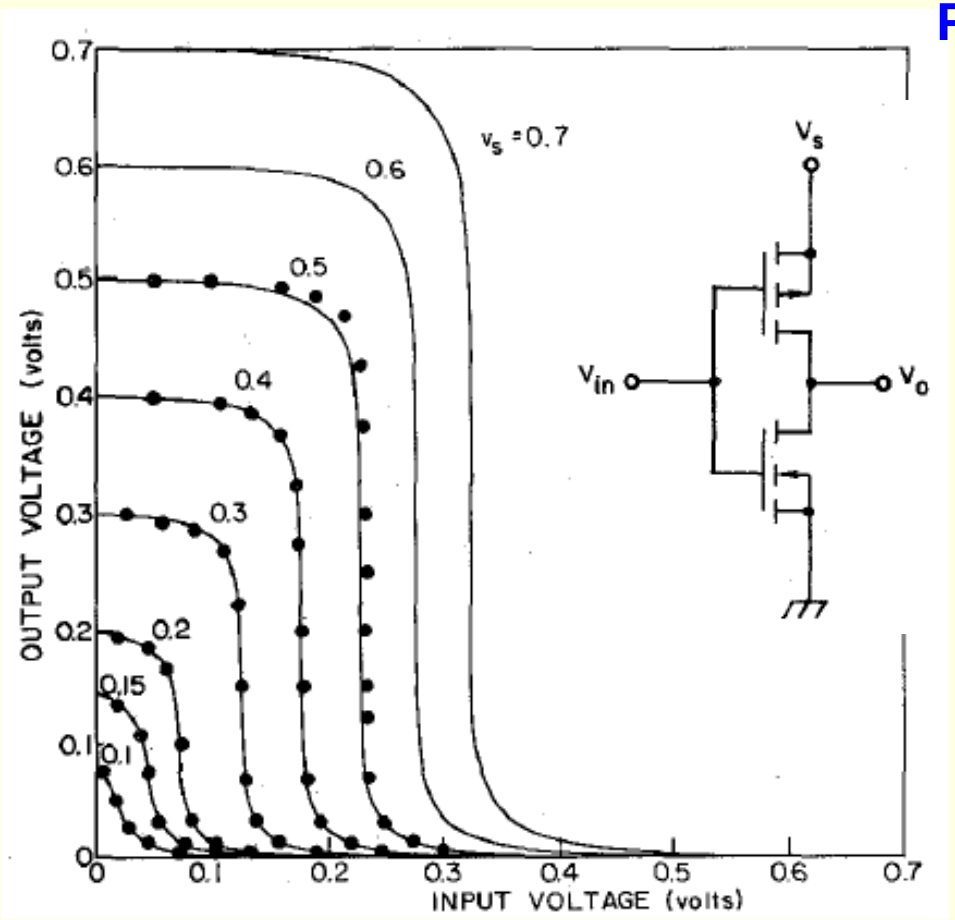


kT/q

There is large room and need for a millivolt switch

Fundamental limits on supply voltage

From device physics - Minimum supply voltage for the standard CMOS inverter



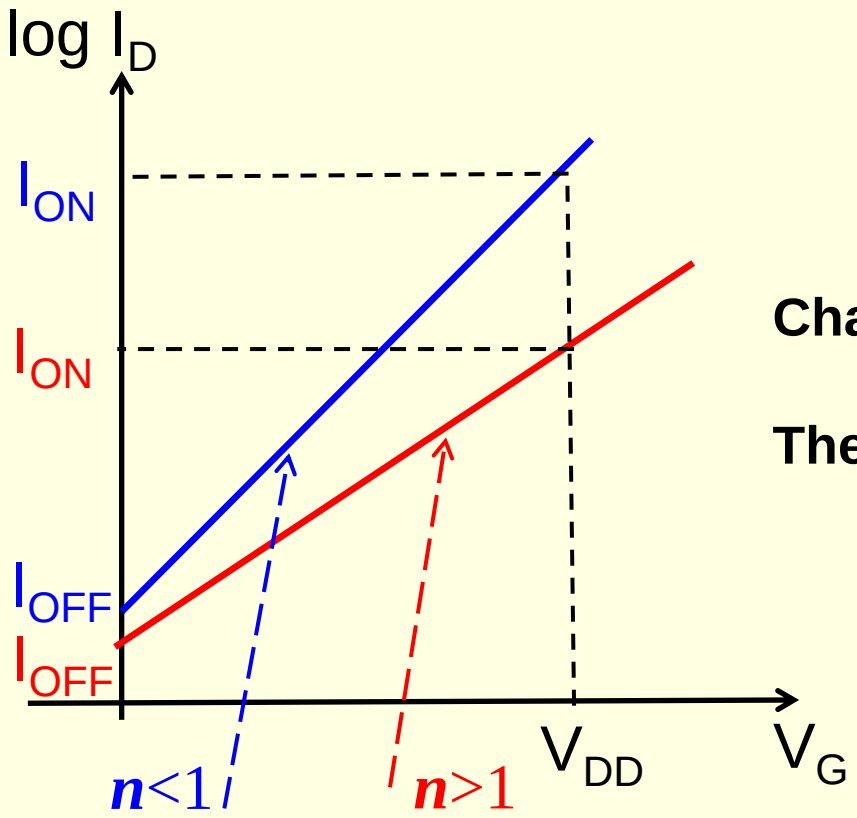
CMOS inverter transfer characteristics
(Swanson and Meindl, IEEE JSSC 1972)

Regenerative logic requires that

$$|\text{Voltage gain}| \geq 1$$

Prof. James Meindl:
Theoretically, the minimum supply voltage for a CMOS inverter is 2 (ln2) (kT/q) = 36 mV at room temperature (IEEE JSSC, 2000)

Searching for the millivolt switch



$$I_D \propto \exp\left(V_G / n\phi_t\right)$$

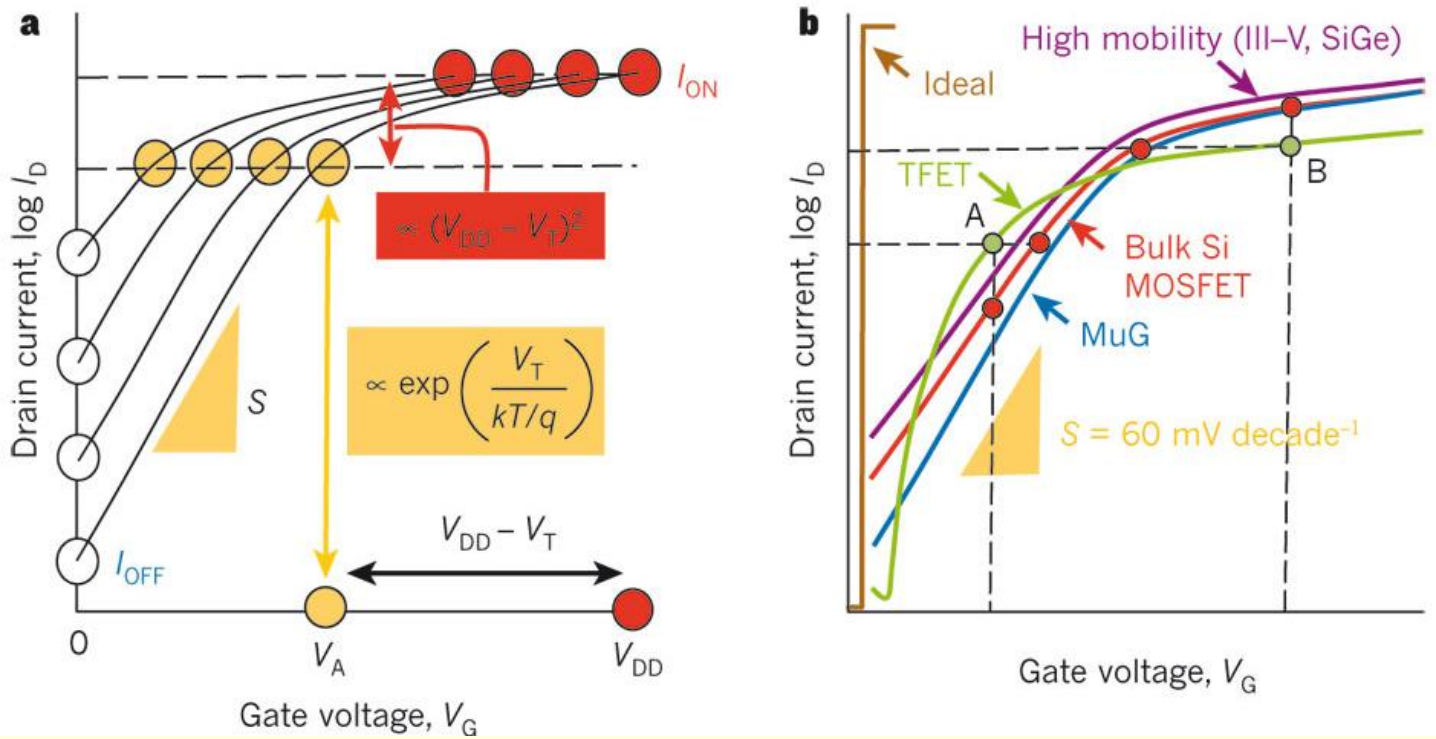
MOSFET $\rightarrow$ $n = 1 + \frac{C_D}{C_{ox}}$

$n<1$ $\quad C_D < 0$???

Change of physical principle:

Thermal injection $\rightarrow$ Tunneling

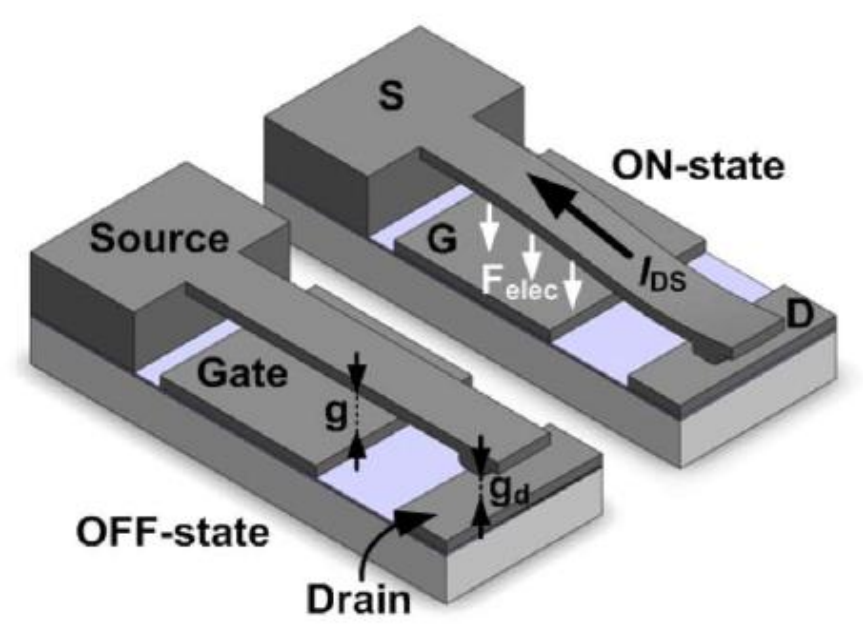
Searching for the millivolt switch



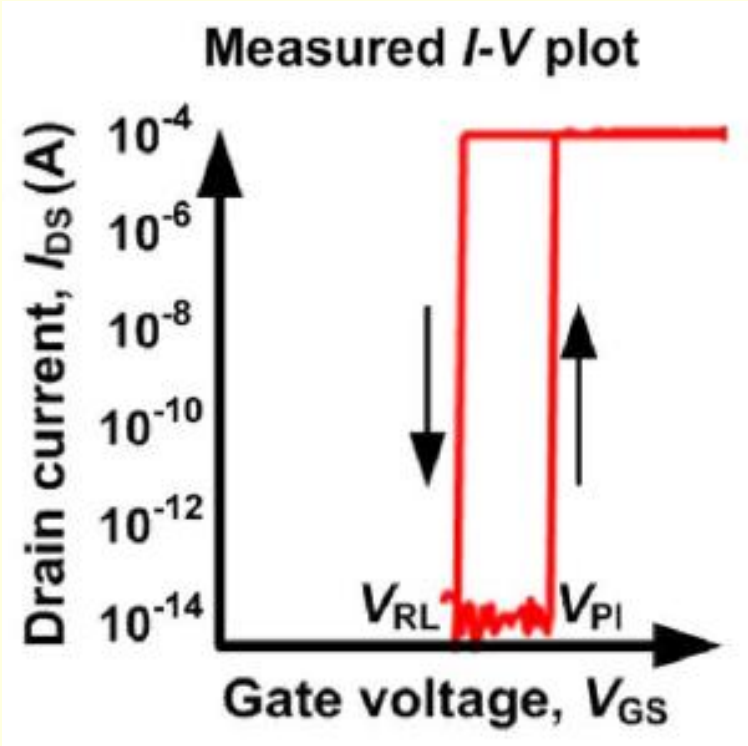
To outperform CMOS transistors, target parameters for Tunnel FETs are:
I_{ON} ~ hundreds of mA;
S_{avg} < 60 mV per decade for five decades of current;
$I_{ON}/I_{OFF} > 10^5$; and $V_{DD} < 0.5$ V.

Ionescu & Riel , Tunnel field-effect transistors as energy-efficient electronic switches, *Nature* 479, 329–337, 2011.

Searching for the millivolt switch

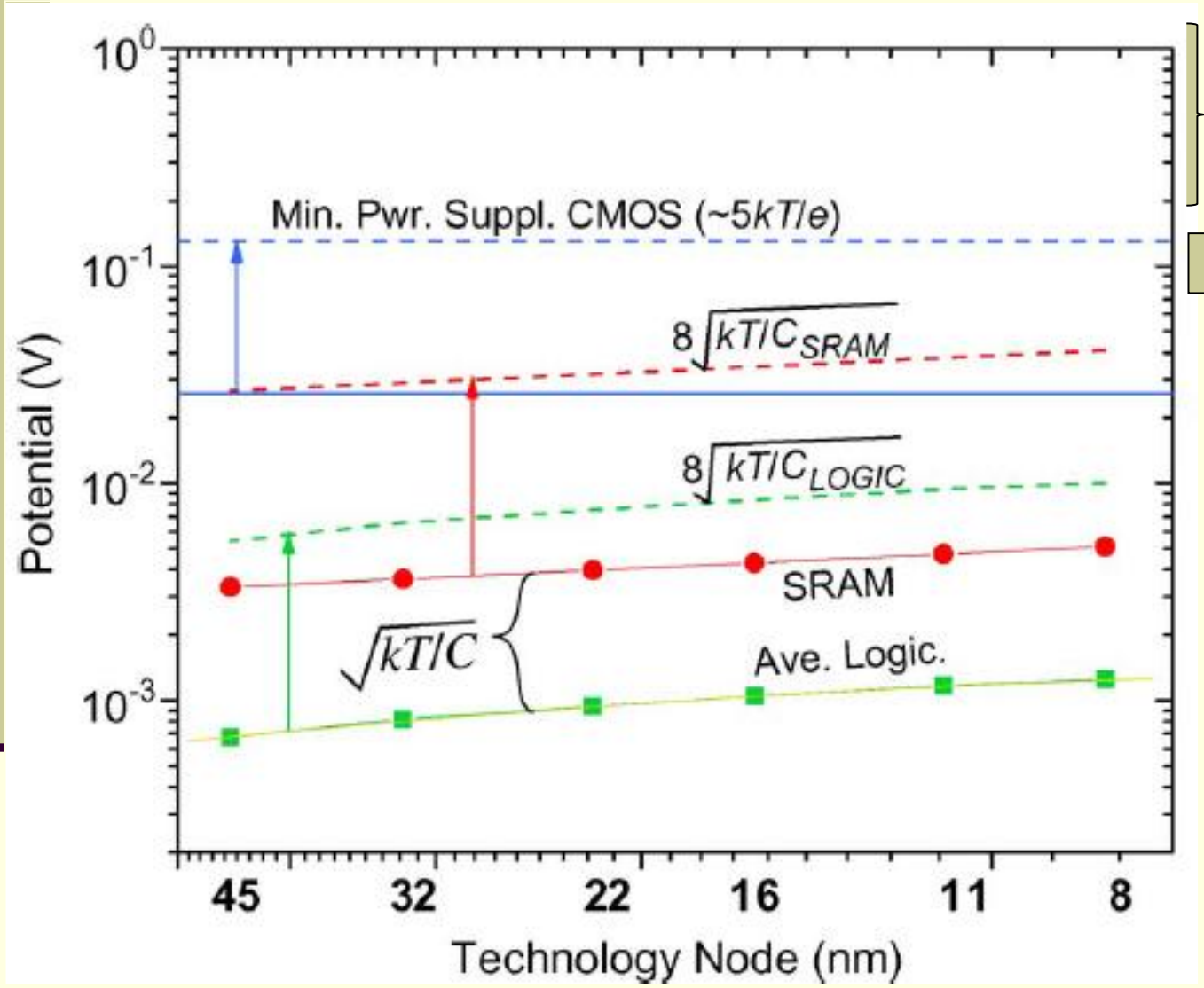


(a) Mechanical switch. When $V_{GS} > V_{PI}$, the electrostatic force is sufficient to bring the source into contact with the drain.



(b) Current versus gate voltage characteristics for a mechanical switch. The switch exhibits a hysteretic switching behavior VRL ≠ VPI

Ultra-low voltage (ULV) CMOS



General purpose analog

Subthreshold logic

Rectifiers/voltage multipliers Colpitts and ring oscillators

Waiting for the beyond CMOS millivolt switch

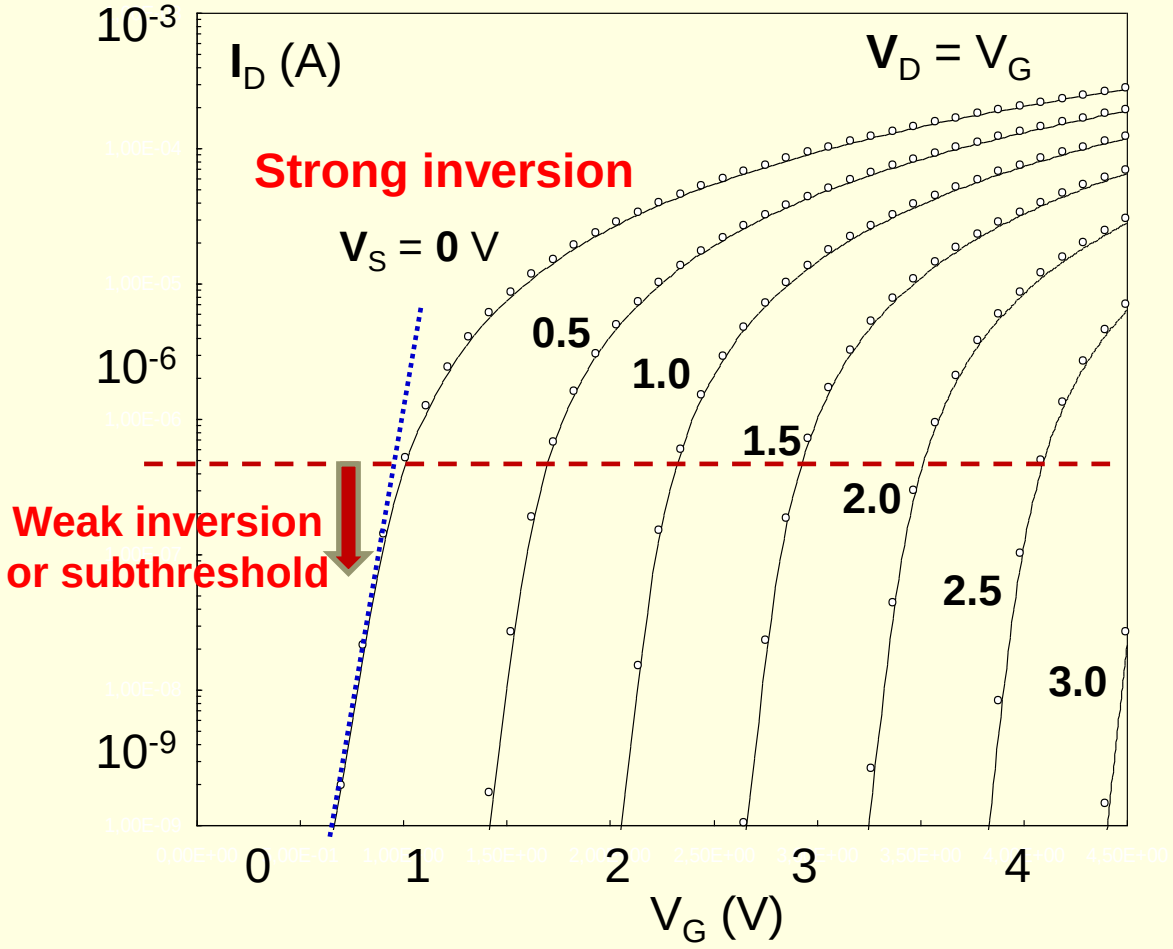
References

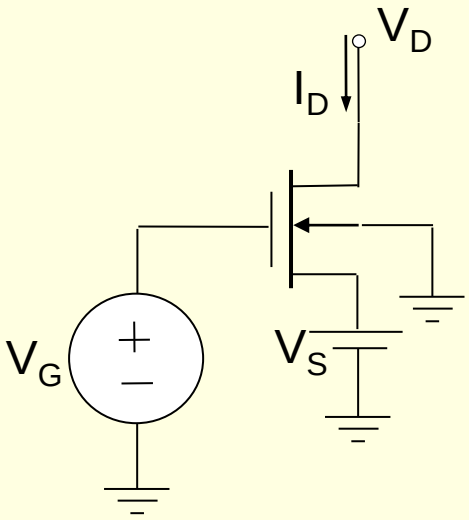
- R. M. Swanson and J. D. Meindl, “Ion-implanted complementary MOS transistors in low voltage circuits,” *IEEE J. Solid State Circuits*, Apr. 1972.
- T. N. Theis and P. Solomon, “In quest of ‘the next switch’: prospects for greatly reduced power dissipation in a successor to the silicon field-effect transistor,” *Proceedings of the IEEE*, Dec. 2010.
- V. Pott *et al.* “Mechanical computing redux: relays for integrated circuit applications,” *Proceedings of the IEEE*, Dec. 2010
- D. Perlmutter, Sustainability in silicon and systems development, *2012 IEEE International Solid-State Circuit Conference*, San Francisco, CA, Feb. 2012.
- R. H. "Dennard, “Past Progress and Future Challenges in LSI Technology", *IEEE Solid-State-Circuits Magazine*, Spring 2015.
- Gordon E. Moore (INTEL), “No exponential is forever” http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=01234194

Chapter 2
Subthreshold MOSFET model

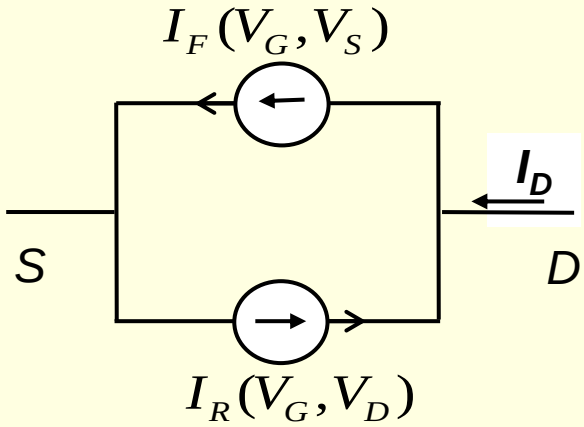
The MOS transistor

Output characteristics @ $V_D=V_G$





Weak inversion (subthreshold) MOSFET model

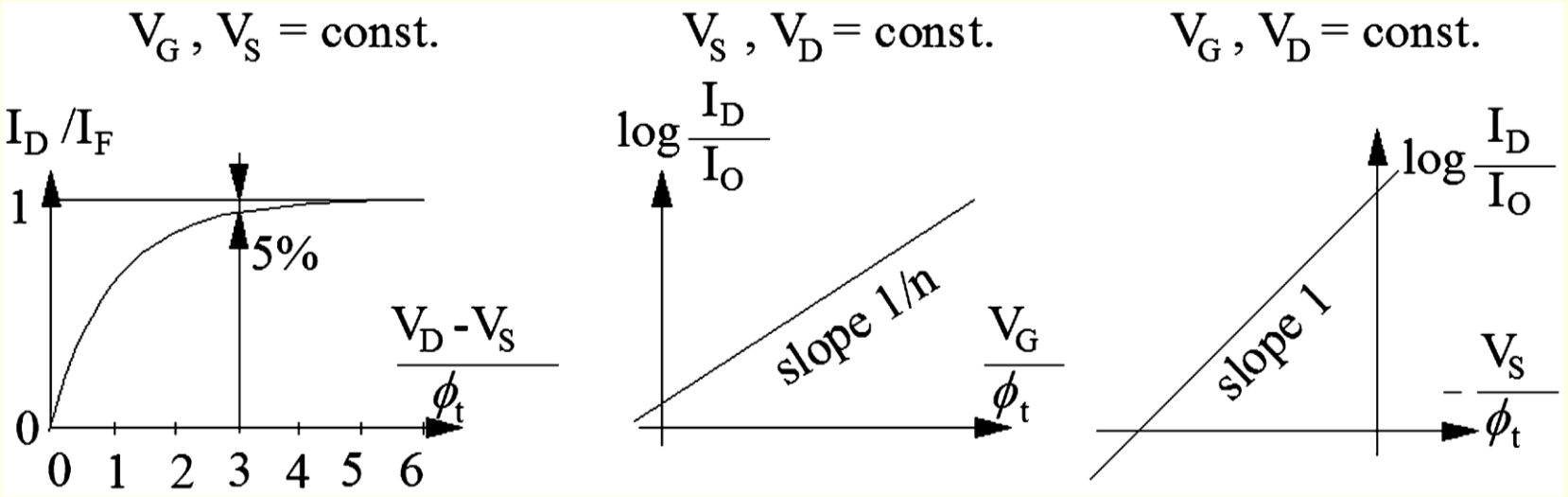


Long-channel model

$$I_{F(R)} = I_0 e^{\frac{V_G - V_{T0}}{n\phi_t} - \frac{V_{S(D)}}{\phi_t}} \qquad I_0 = \mu \frac{W}{L} n C'_{ox} \phi_t^2 e^1$$

$$n = 1 + \frac{C_D}{C_{ox}} \qquad \phi_t = \frac{kT}{q} (\approx 26 \text{ mV} @ 300\text{K})$$

$$I_D = I_F - I_R = I_0 e^{\left(\frac{V_G - V_{T0}}{n} - V_S\right)/\phi_t} \left[1 - e^{-V_{DS}/\phi_t}\right]$$



Low-frequency small-signal model in weak inversion

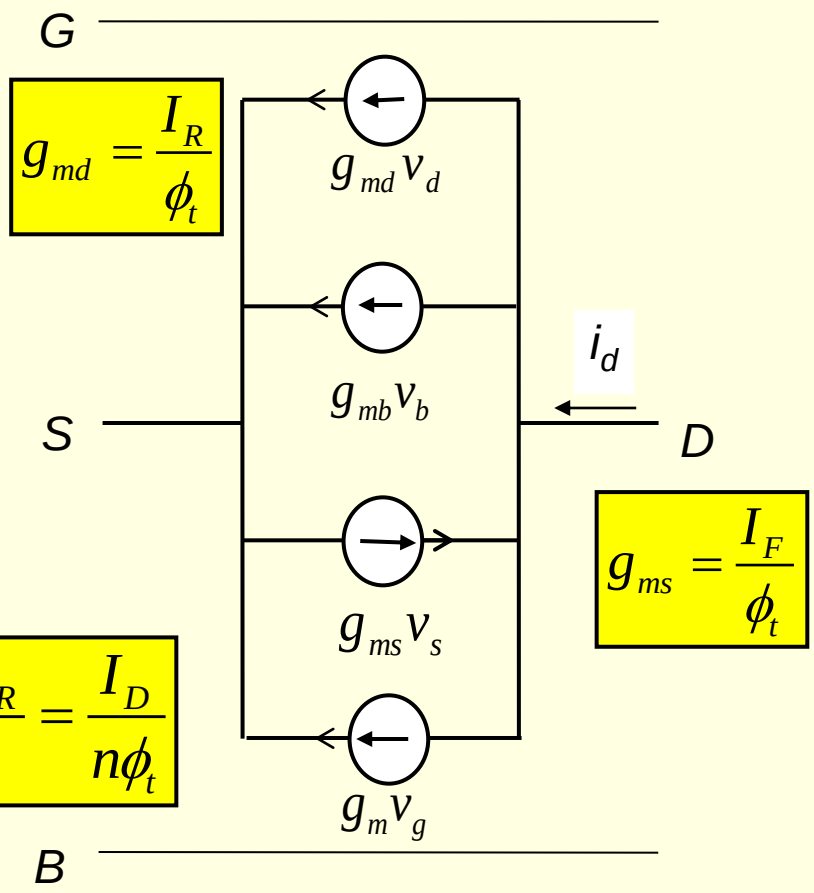
Transconductances

$$\Delta I_D = g_{mg}\Delta V_G - g_{ms}\Delta V_S + g_{md}\Delta V_D + g_{mb}\Delta V_B$$

$$g_{mg} - g_{ms} + g_{md} + g_{mb} = 0$$

$$g_{mg} = \frac{\partial I_D}{\partial V_G}, g_{ms} = -\frac{\partial I_D}{\partial V_S},$$

$$g_{md} = \frac{\partial I_D}{\partial V_D}, g_{mb} = \frac{\partial I_D}{\partial V_B}$$

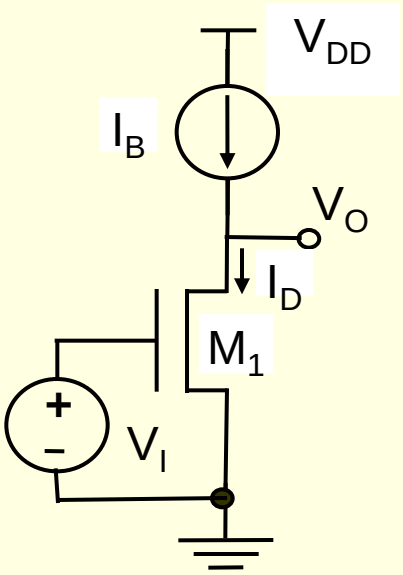


$$g_m = \frac{g_{ms} - g_{md}}{n} = \frac{I_F - I_R}{n\phi_t} = \frac{I_D}{n\phi_t}$$

Low-voltage operation of the common-source amplifier

Intrinsic gain stage

(I_B ideal current source)

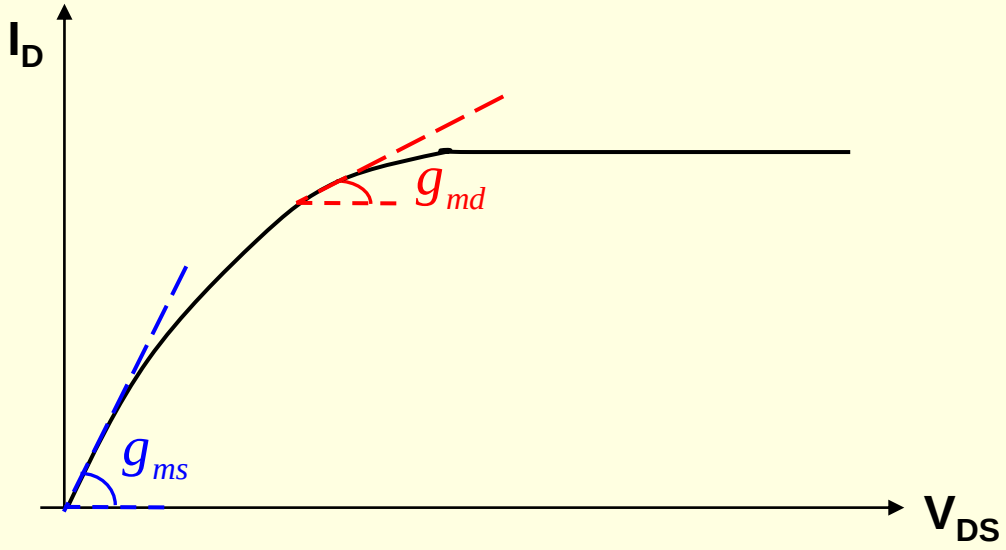


$$|A_V| = \frac{g_m}{g_{md}} = \frac{g_{ms} - g_{md}}{n g_{md}} = \frac{1}{n}\left(\frac{g_{ms}}{g_{md}} - 1\right)$$

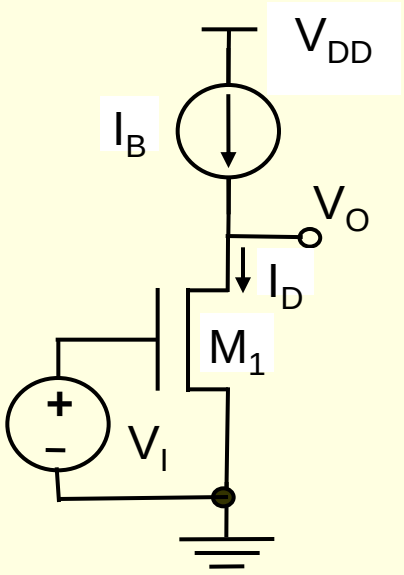
weak inversion operation

$$\frac{g_{ms}}{g_{md}} = e^{\frac{V_{DS}}{\phi_t}}$$

$$g_{ms} = g_{md} \ @ \ V_{DS} = 0$$



Low-voltage operation of the common-source amplifier



$$|A_V| = \frac{g_m}{g_{md}} = \frac{g_{ms} - g_{md}}{n g_{md}} = \frac{1}{n}\left(\frac{g_{ms}}{g_{md}} - 1\right) \qquad \frac{g_{ms}}{g_{md}} = e^{\frac{V_{DS}}{\phi_t}}$$

$$|A_V| = \frac{1}{n}\left(e^{\frac{V_{DS}}{\phi_t}} - 1\right)$$

or

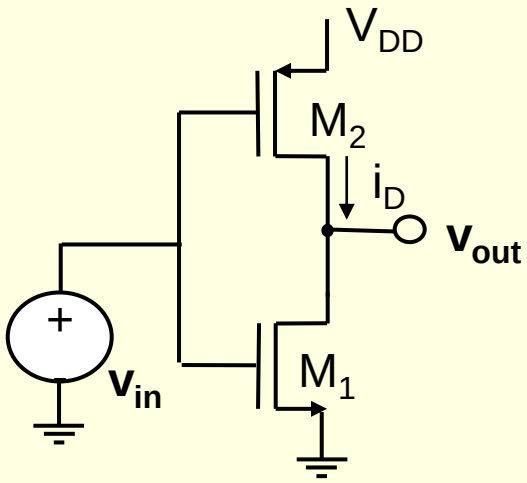
$$V_{DS} = \phi_t \ln\left(1 + n|A_V|\right)$$

$$V_{DS} = \phi_t \ln\left(1 + n|A_V|\right)$$

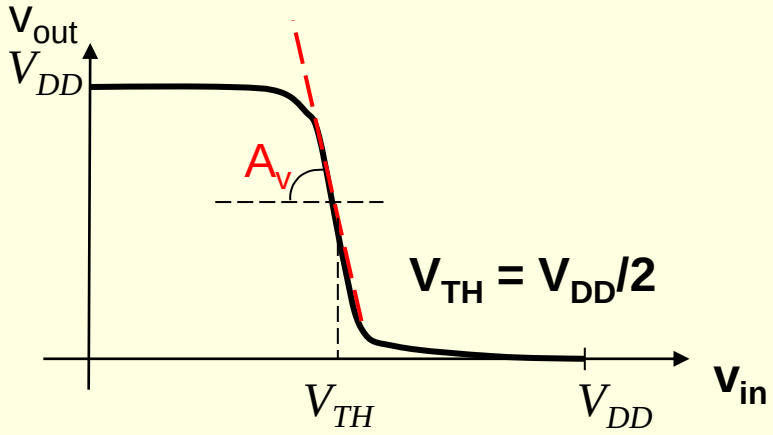
$$V_{DS} = \phi_t \ln(2) \quad \text{for } n = |A_V| = 1$$

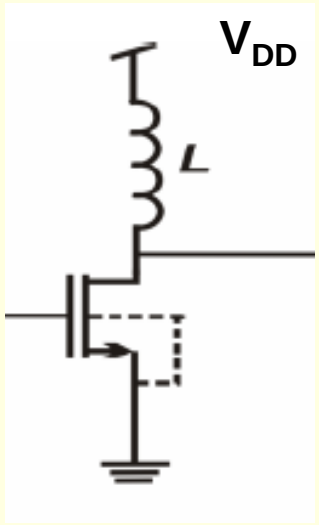
Low–voltage operation of the CMOS inverter

Minimum supply voltage for amplification $|A_V| = 1$



'ideal' MOSFET *n* = 1





$$V_{DS} = \phi_t \ln\left(1 + n|A_V|\right)$$

$$V_{DS} = V_{DD}$$

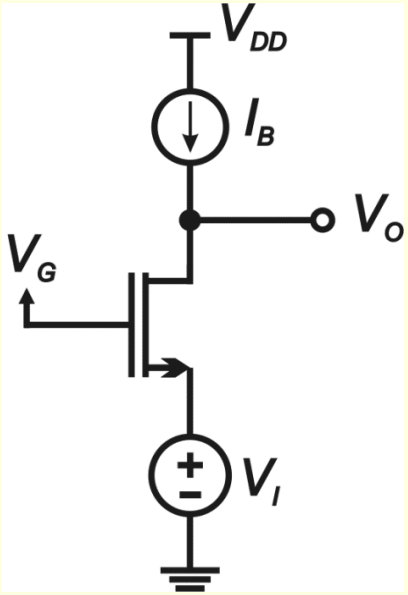
$$V_{DD\min} = (\ln 2)\phi_t$$

$$V_{DS} = V_{DD}/2$$

$$V_{DD\min} = 2(\ln 2)\phi_t$$

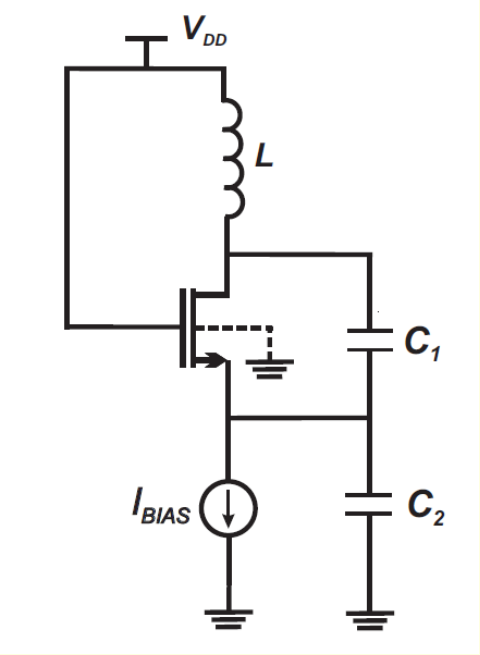
J. Meindl, IEEE JSSC, 2000

Low-voltage operation of the common-gate amplifier



$$A_{v,cg} = \frac{v_o}{v_i} = \frac{g_{ms}}{g_{md}} = e^{\frac{qV_{DS}}{kT}}$$

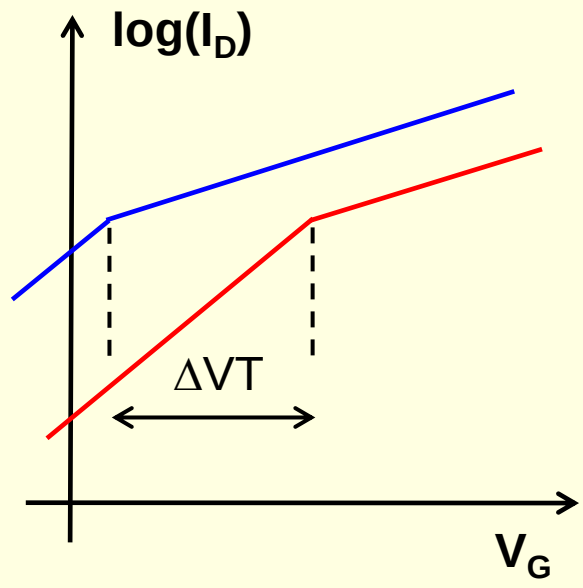
The common-gate amplifier provides a voltage gain of greater than unity for V_{DS}>0. → Very useful property for lowering the supply voltage limit for the operation of oscillators (later).

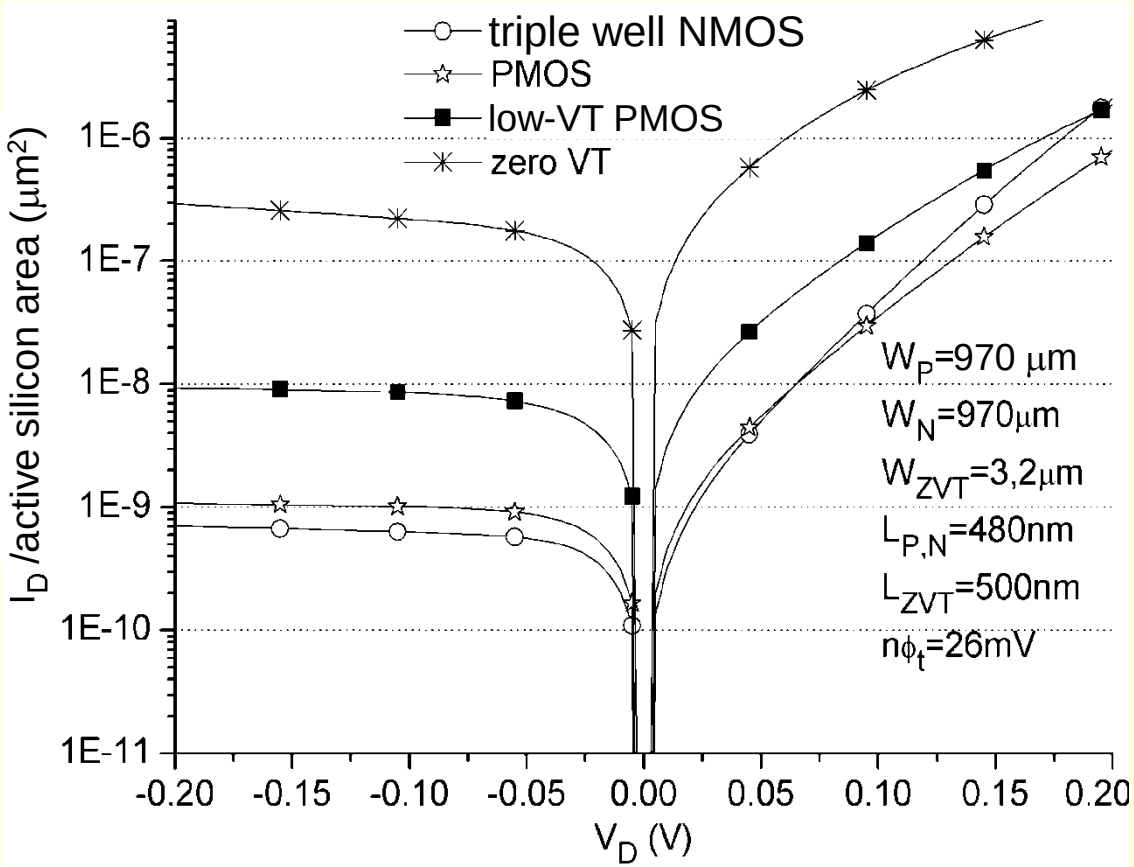


Common- gate Colpitts oscillator

Zero-VT MOSFETs

1 – high current/unit area for low voltages

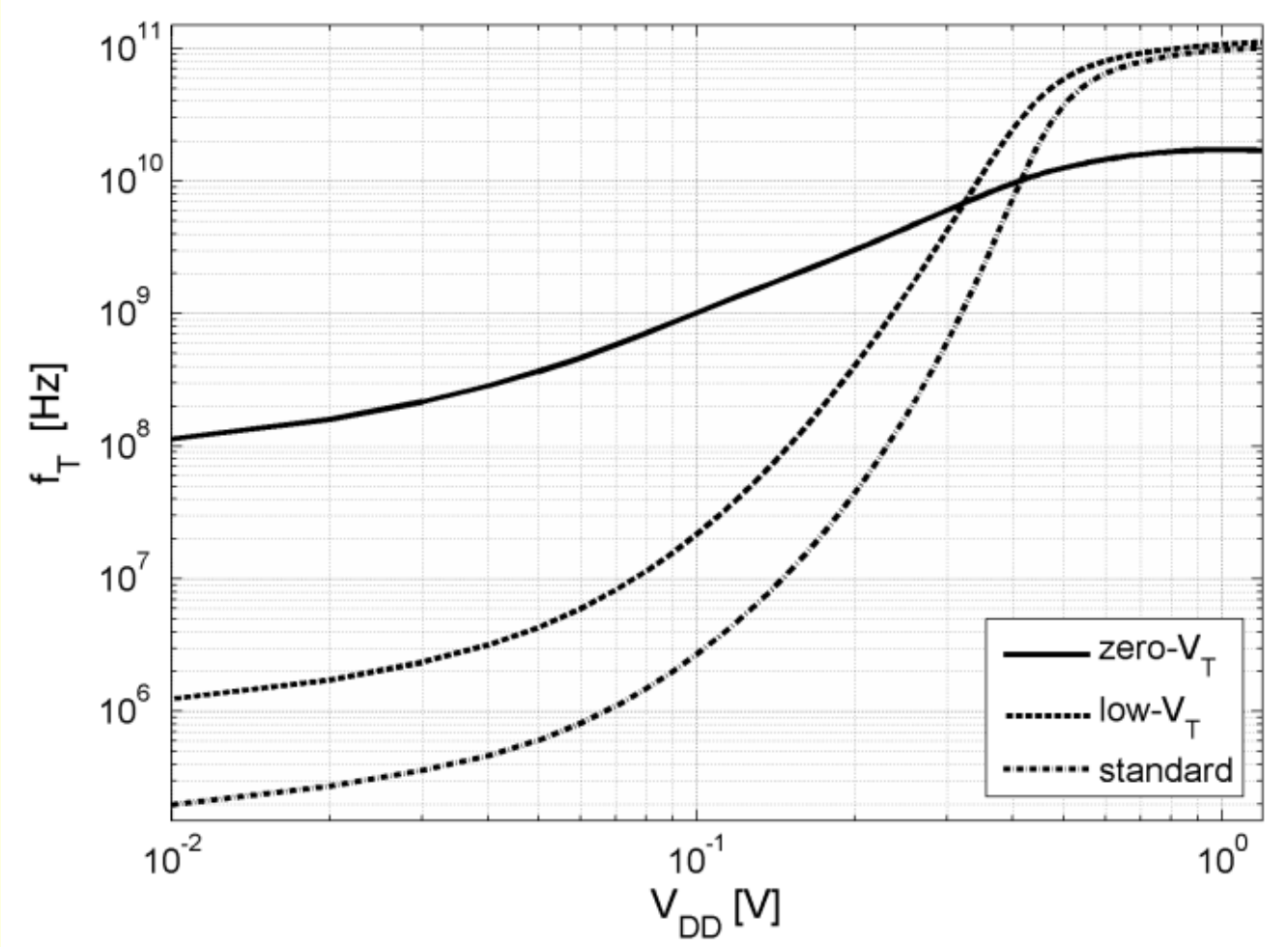




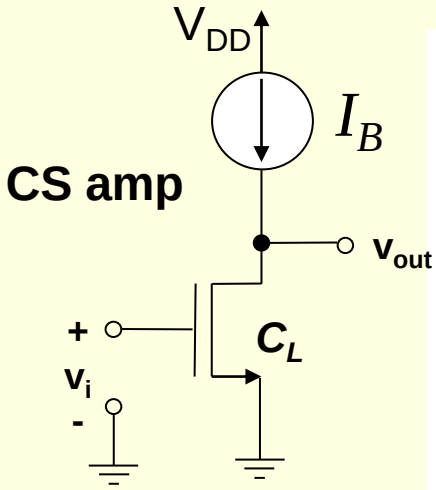
I-V characteristics of diode-connected MOSFETs (IBM 130nm)

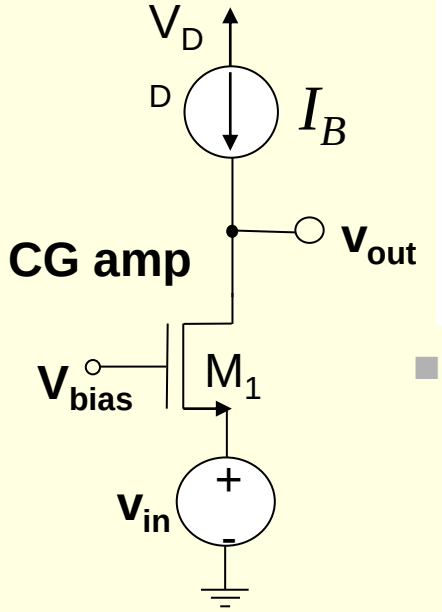
Zero-VT MOSFETs

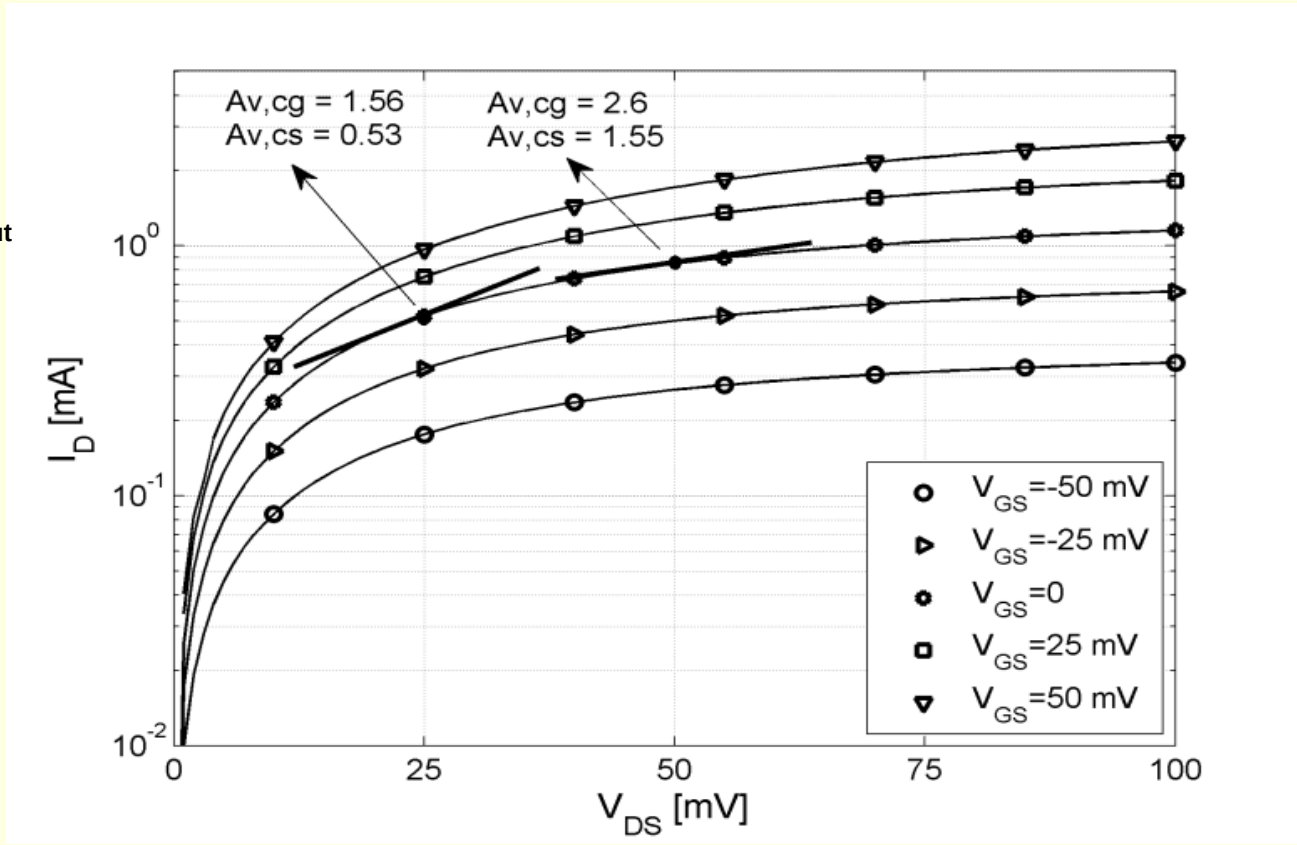
2 – high g_m/C (f_T) for low voltages



Zero-VT MOSFETs







- I_D x V_{DS} (V_S=V_B) characteristics for a zero-VT transistor with W/L=2500µm/420nm. For V_{GS}= 0 V and V_{DS}= 25 mV the values of the common-gate and common-source gains are 1.56 and 0.53, respectively (moderate inversion operation).

References

- R. M. Swanson and J. D. Meindl, “Ion-implanted complementary MOS transistors in low voltage circuits,” *IEEE J. Solid State Circuits*, vol. 7, pp. 146-153, Apr. 1972.
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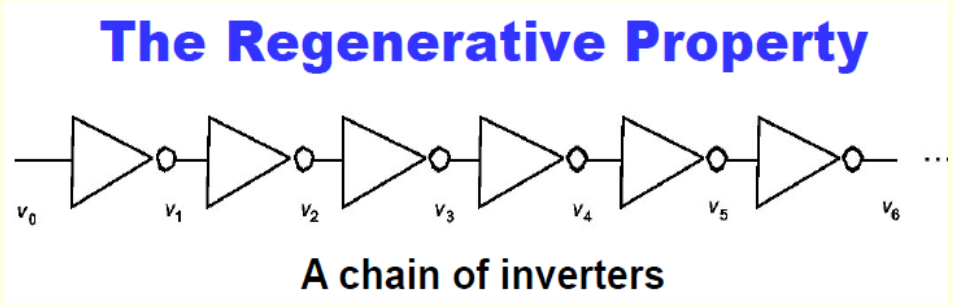
- Márcio Cherem Schneider and Carlos Galup-Montoro, *CMOS Analog Design Using All-Region MOSFET Modeling*, Cambridge University Press, 2010.

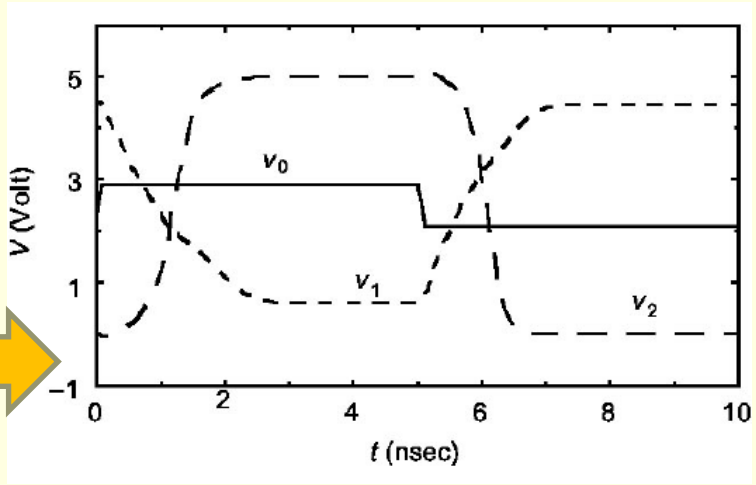
Chapter 3
Subthreshold CMOS logic and Schmitt trigger

Regenerative Property

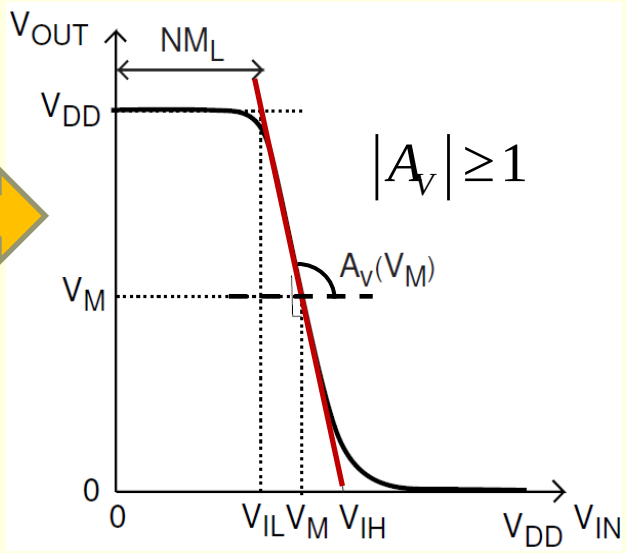
What´s the minimum supply voltage for "correct" operation?



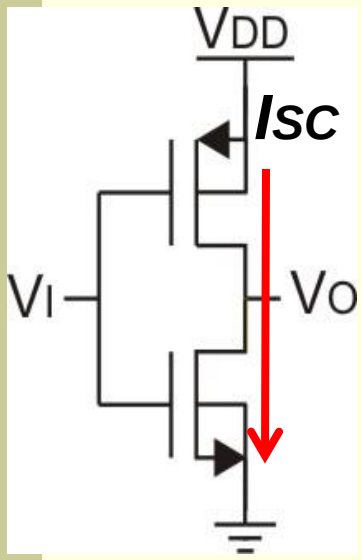
Regenerative property: a disturbed signal gradually converges back to V_{OL} or V_{OH} after passing a number of logical stages.

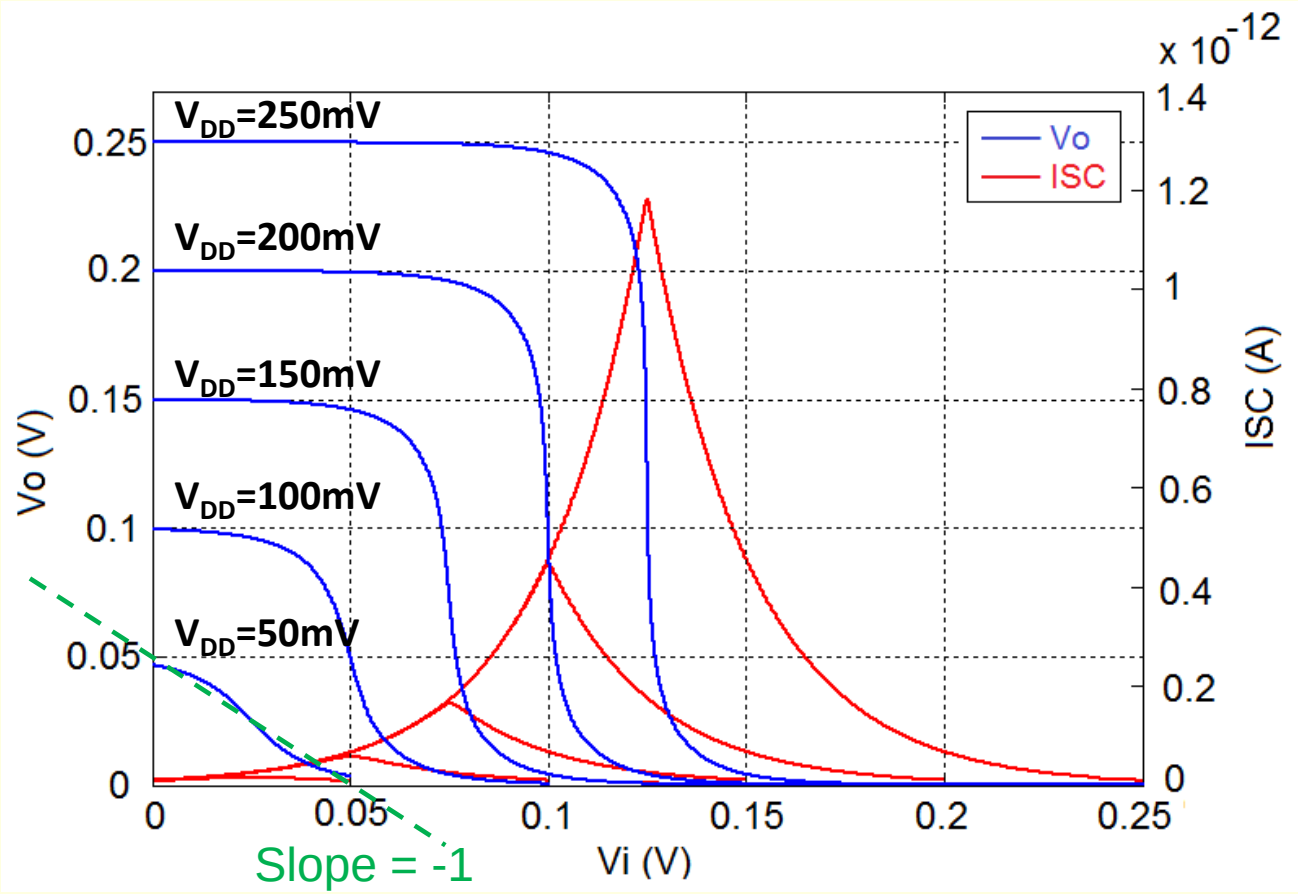


To be regenerative the VTC must present voltage gain greater than 1 in absolute value



THE CMOS INVERTER IN WEAK INVERSION - 1





Note that:

VDD	VoH (Vi = 0)	VoL (Vi = VDD)
200 mV	200 mV	0mV
50 mV	46.6 mV	3.4mV

THE CMOS INVERTER IN WEAK INVERSION - 2

In the ideal case of NMOS and PMOS transistors with the same strength

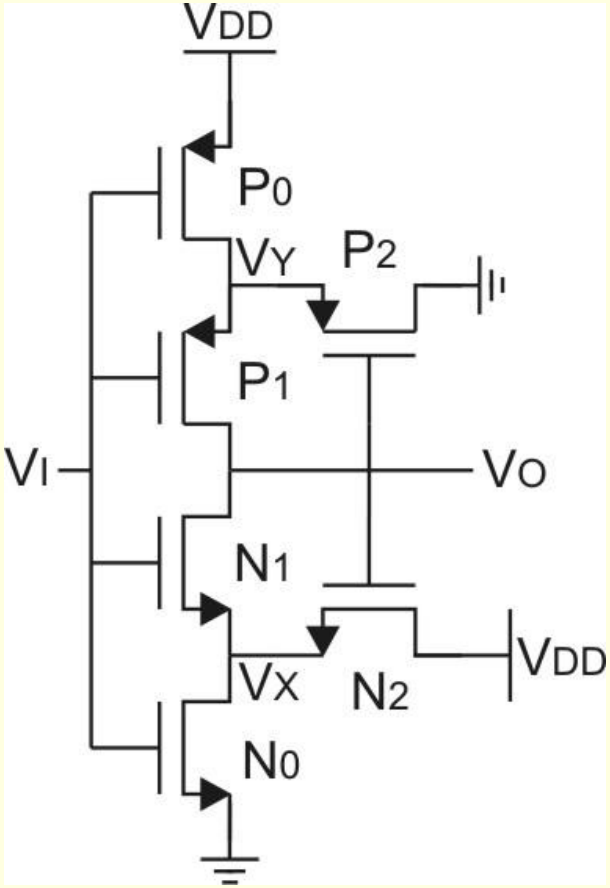
$$\left|\frac{dV_O}{dV_I}\right|_{V_O=\frac{V_{DD}}{2}} = \frac{e^{\frac{V_{DD}}{2\cdot\phi_t}}-1}{n}$$

- The minimum operating supply voltage of the inverter and any CMOS static logic gate must be at least equal to unity, *i.e.*

$$\left|\frac{dV_O}{dV_I}\right|_{V_O=\frac{V_{DD}}{2}} = 1 \qquad \left|\frac{dV_O}{dV_I}\right|_{V_O=\frac{V_{DD}}{2}} = \frac{e^{\frac{V_{DD}}{2\cdot\phi_t}}-1}{n}$$

$$V_{DD\min} = 2\phi_t \ln(2) = 36\text{mV at } 300\text{K} \qquad \textit{for } n\text{=1}$$

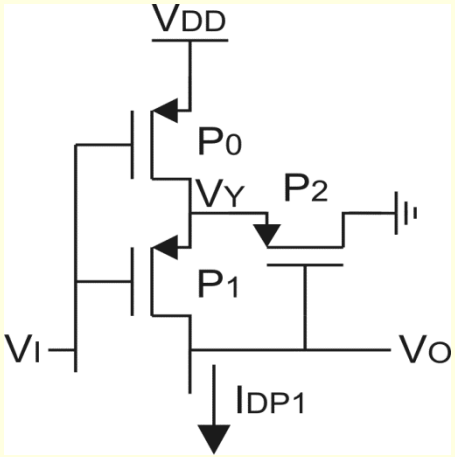
6-T Schmitt trigger - 1

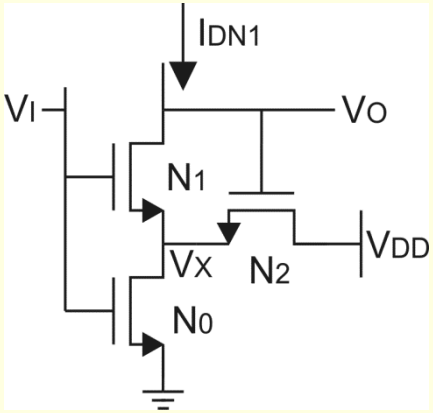


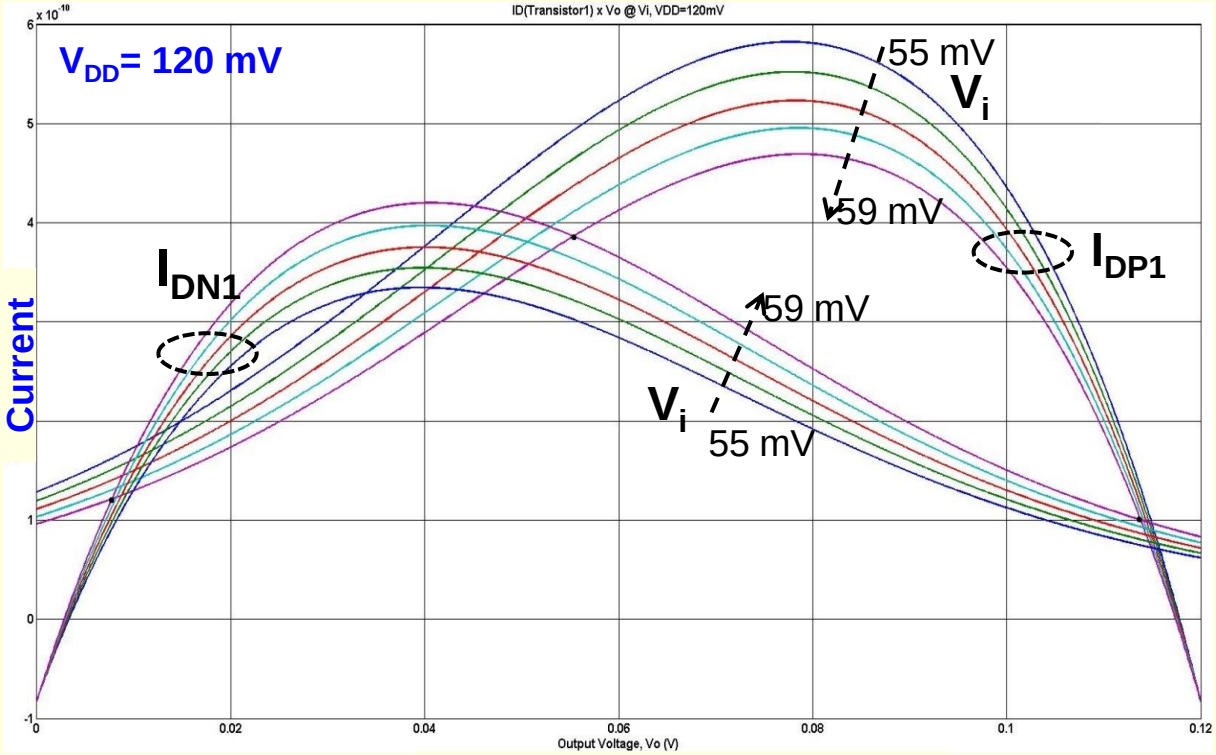
- *2 internal nodes (VX and VY)*
- *Feedback transistors (P2/N2) controlled by the output*
- *Hysteresis dependent on VDD & relative transistor strength*
- *Modeled in strong inversion but not in weak inversion*
- *For symmetric operation, corresponding NMOS and PMOS MOSFETs have the same current capability.*

6-transistor (6-T) Schmitt Trigger

6-T Schmitt trigger - 2

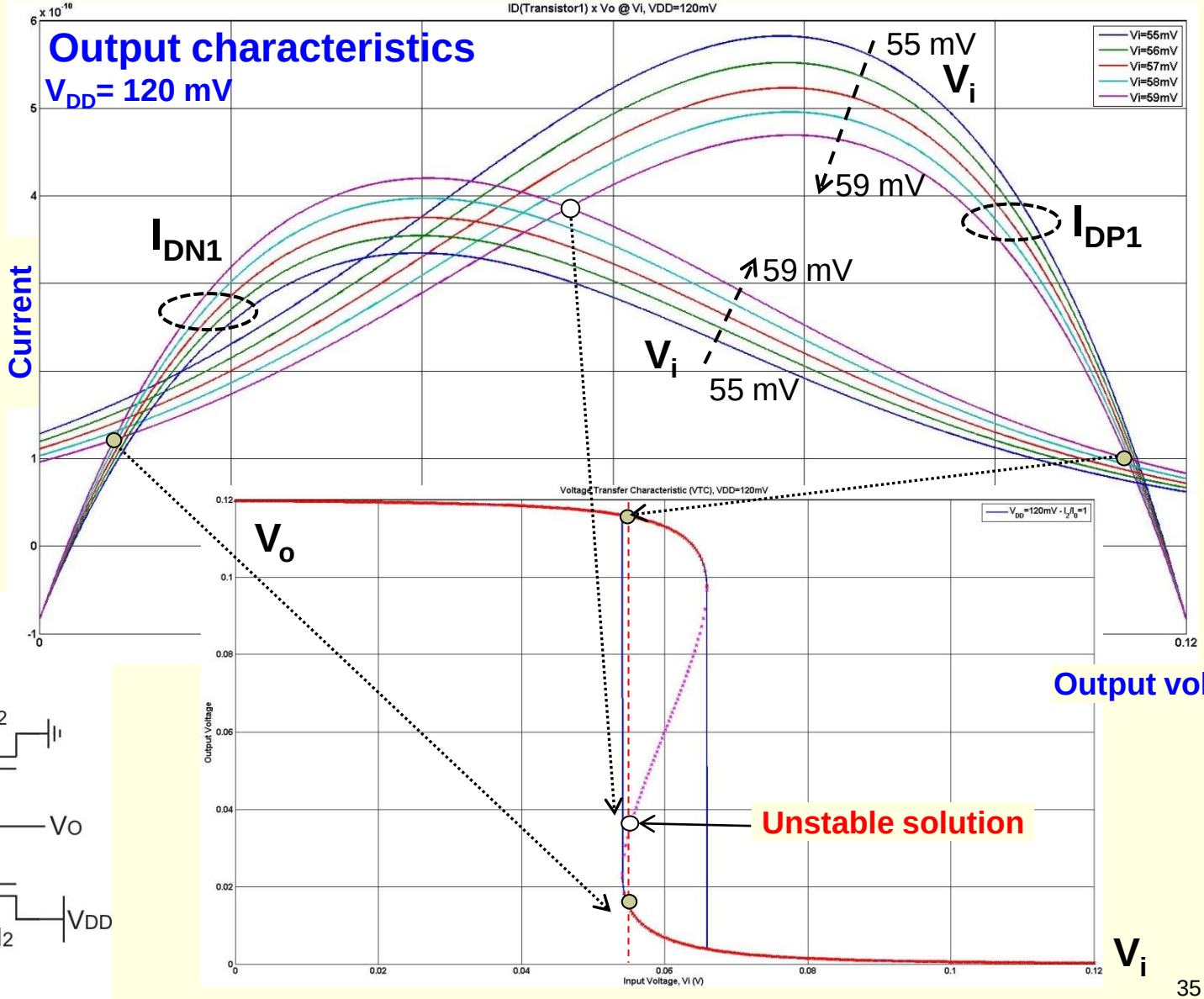


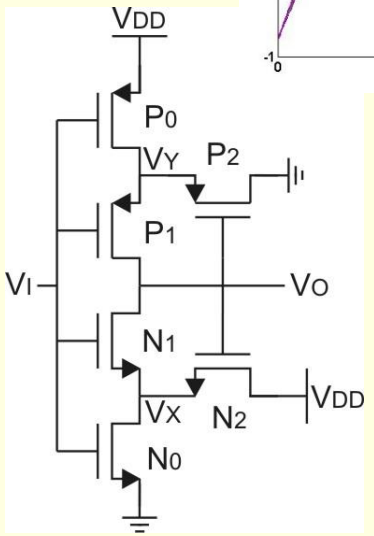




Output characteristics of N and P networks

6-T Schmitt trigger - 3



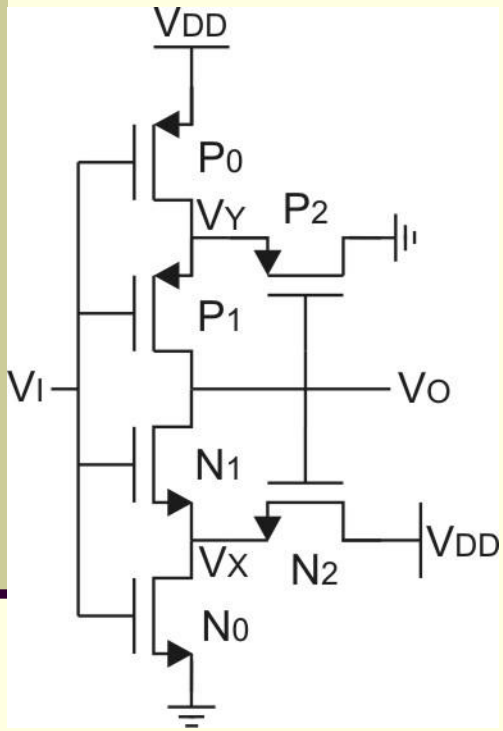


6-T Schmitt trigger - 4

KCL for V_x, V_y, V_o

Symmetric ST $n_N = n_P = 1$, $V_{TN} = |V_{TP}|$,

$I_{N0} = I_{P0} = I_0$, $I_{N1} = I_{P1} = I_1$, $I_{N2} = I_{P2} = I_2$



Loop to solve numerically

$$e^{\frac{V_Y}{\phi_t}} = \frac{I_0 \cdot e^{\frac{V_{DD}}{\phi_t}} + I_1 \cdot e^{\frac{V_O}{\phi_t}} + I_2 \cdot e^{\frac{V_I - V_O}{\phi_t}}}{I_0 + I_1 + I_2 \cdot e^{\frac{V_I - V_O}{\phi_t}}}$$

$$e^{\frac{V_I - V_X}{\phi_t}} - e^{\frac{V_I - V_O}{\phi_t}} = e^{\frac{V_Y - V_I}{\phi_t}} - e^{\frac{V_O - V_I}{\phi_t}}$$

$$e^{\frac{V_X}{\phi_t}} = \frac{I_0 + I_1 + I_2 \cdot e^{\frac{V_O - V_I}{\phi_t}}}{I_0 + I_1 \cdot e^{\frac{-V_O}{\phi_t}} + I_2 \cdot e^{\frac{V_O - V_I}{\phi_t}} \cdot e^{\frac{-V_{DD}}{\phi_t}}}$$

P-network

$I_{DP0}=I_{DP1}+I_{DP2}$

$I_{DP1}=I_{DN1}$

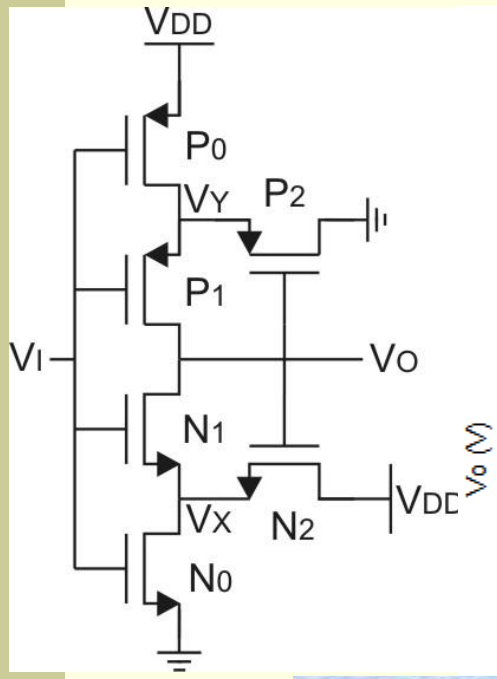
N-network

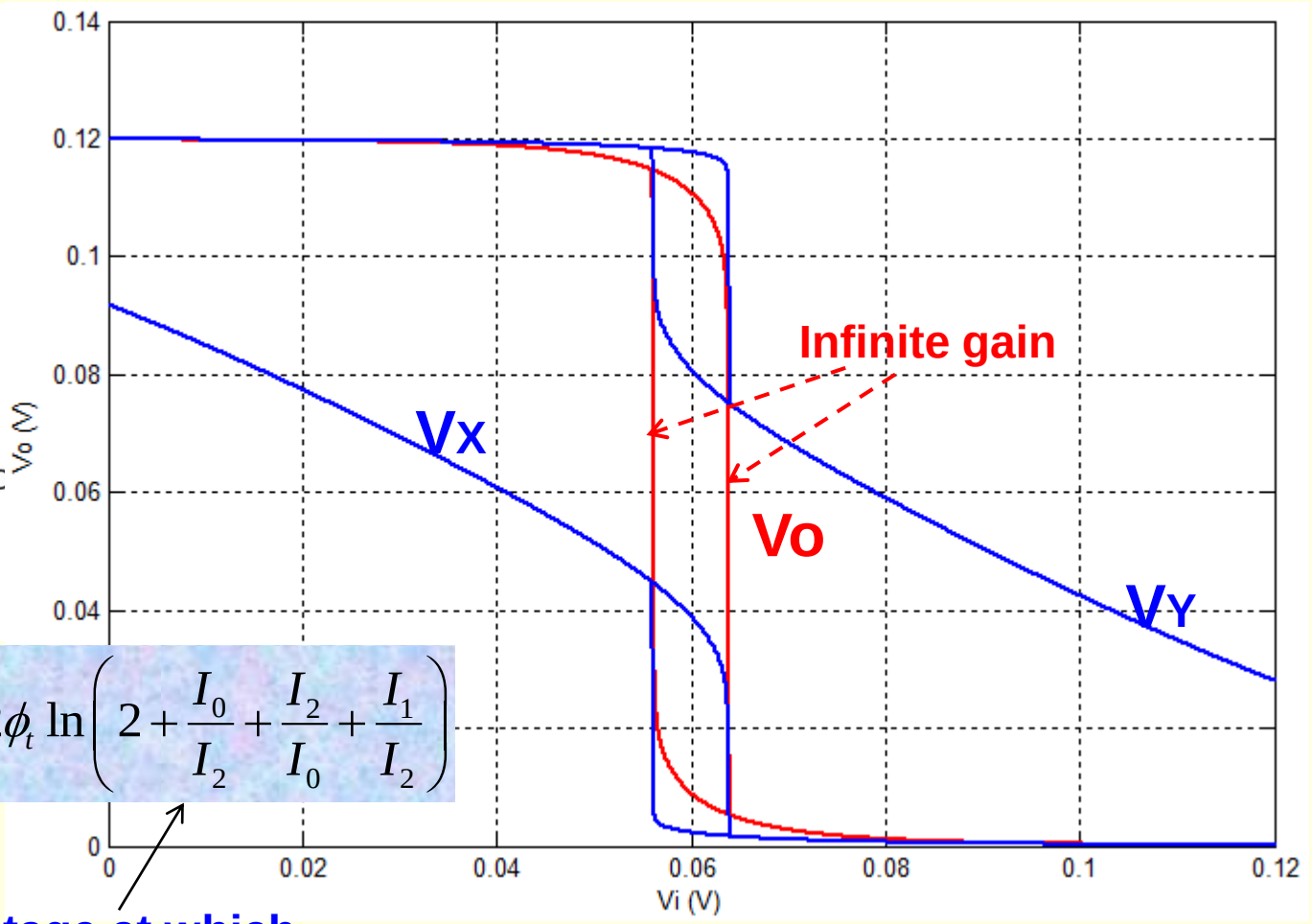
$I_{DN0}=I_{DN1}+I_{DN2}$

$$I_{N(P)} = I_{ON(P)} \cdot e^{\frac{-|V_{TN(P)}|}{n_{N(P)} \cdot \phi_t}}$$

6-T Schmitt trigger - 5

$I_0 = I_1 = I_2 = 1$ nA , $V_{DD} = 120$ mV

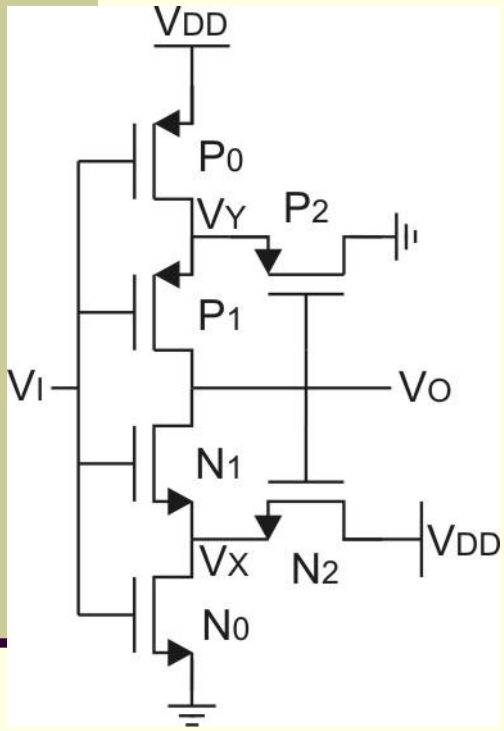


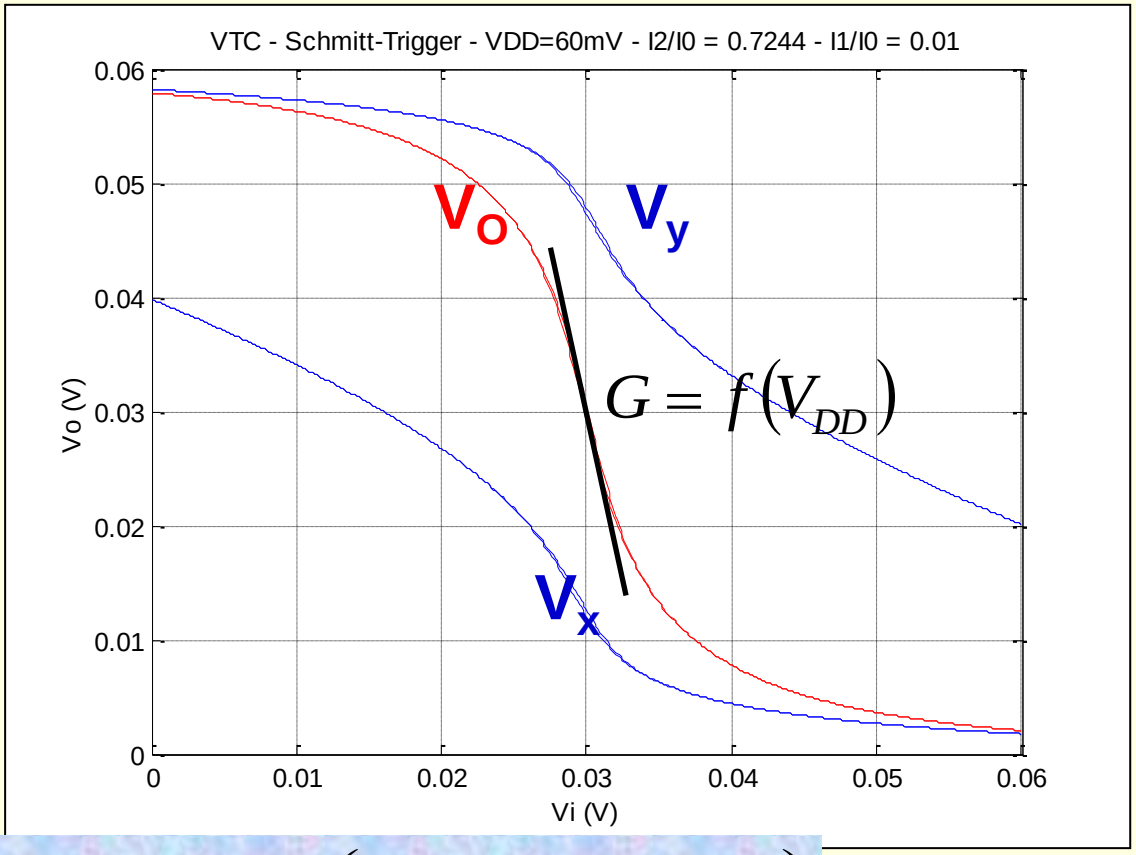


$$V_{DD} > 2\phi_t \ln\left(2 + \frac{I_0}{I_2} + \frac{I_2}{I_0} + \frac{I_1}{I_2}\right)$$

Supply voltage at which hysteresis starts to appear

6-T Schmitt trigger - 6

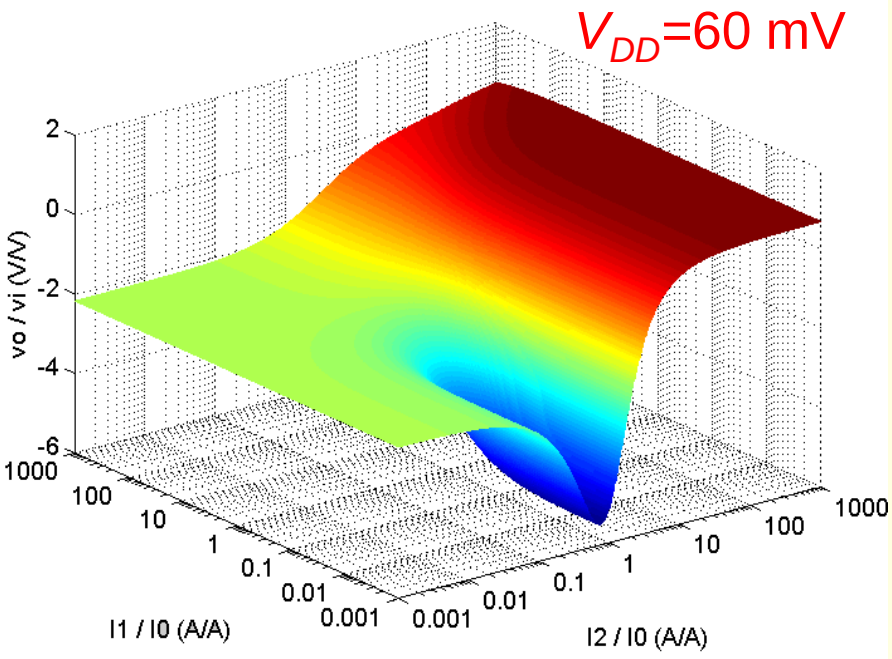




$$V_{DD} < 2\phi_t \ln\left(2 + \frac{I_0}{I_2} + \frac{I_2}{I_0} + \frac{I_1}{I_2}\right)$$

No hysteresis

6-T Schmitt trigger - 7



V_{DD} (mV)	I_2/I_0 opt (A/A)	ST Gain	St. Inv. Gain
70	0.91	-18.6	-2.86
65	0.81	-9.00	-2.51
60	0.73	-5.47	-2.18
55	0.65	-3.76	-1.89
50	0.58	-2.73	-1.63
45	0.50	-2.05	-1.38
40	0.44	-1.56	-1.16
35	0.39	-1.20	-0.97
31.5	0.33	-1.00	-0.84

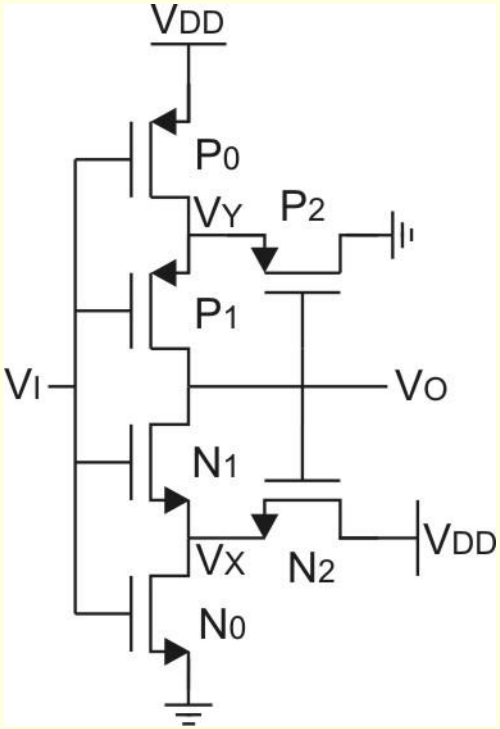
$$\left.\frac{I_1}{I_0}\right|_{OPTIMUM} = 0$$

$$\left.\frac{I_2}{I_0}\right|_{OPTIMUM} = \frac{\sqrt{1+e^{\frac{V_{DD}}{2\phi_t}} - e^{-\frac{V_{DD}}{2\phi_t}}} - 1}{1+e^{-\frac{V_{DD}}{2\phi_t}}}$$

Strength ratios for highest gain for a given V_{DD}

6-T Schmitt trigger - 8

What is the minimum operating voltage that results in gain = -1 ?

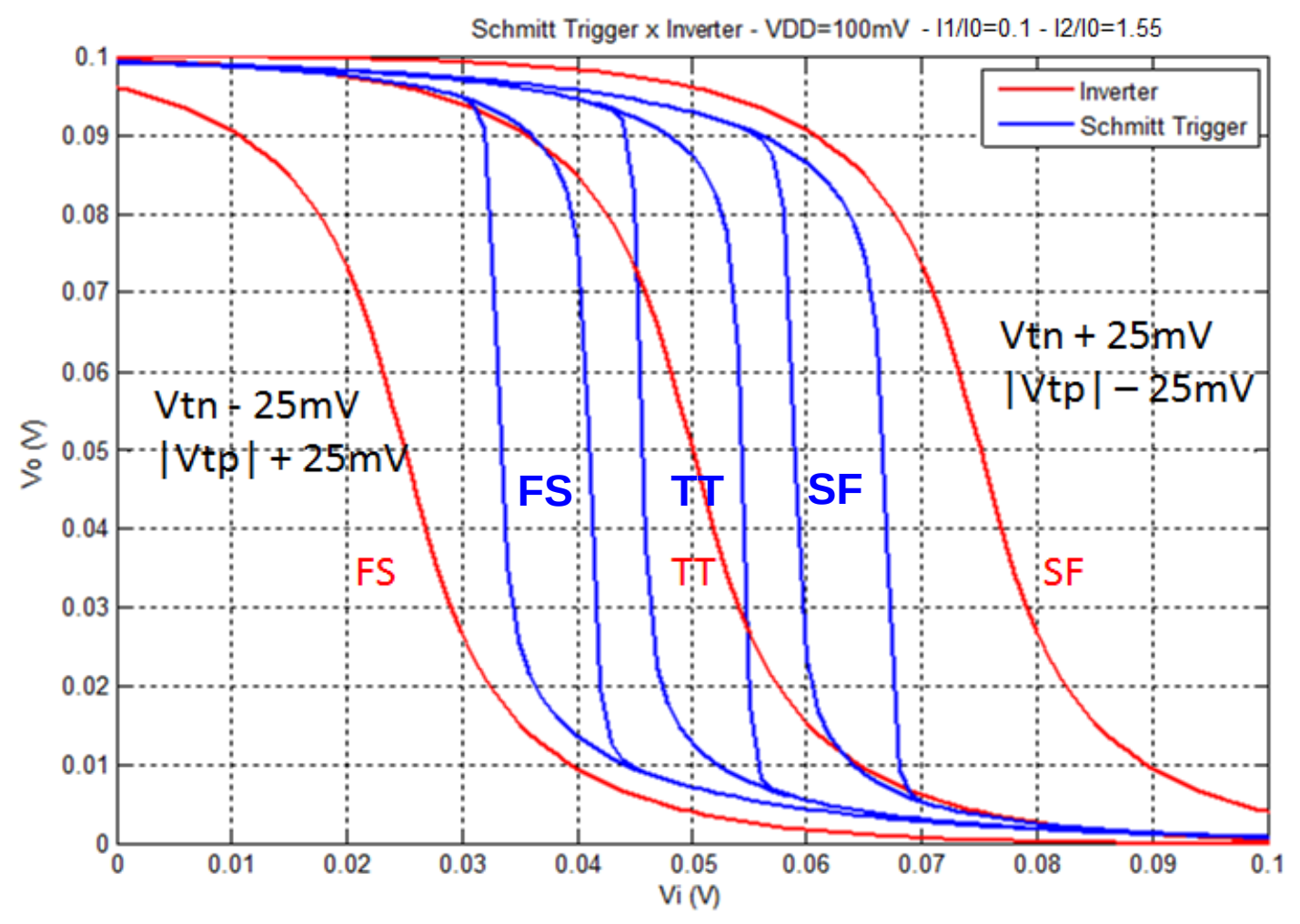


$$V_{DD\min} = 2\phi_t \ln\left(\frac{1}{\sqrt{73}-8}\right) = 31.5\text{mV at } 300\text{K}$$

73 is the best number !

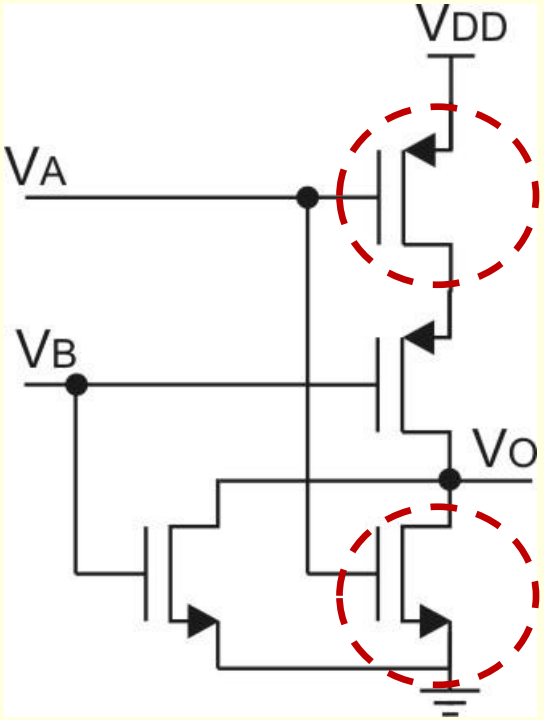
6-T Schmitt trigger - 9

ST inverter is less sensitive to process parameter (V_T) spreading than the standard inverter.

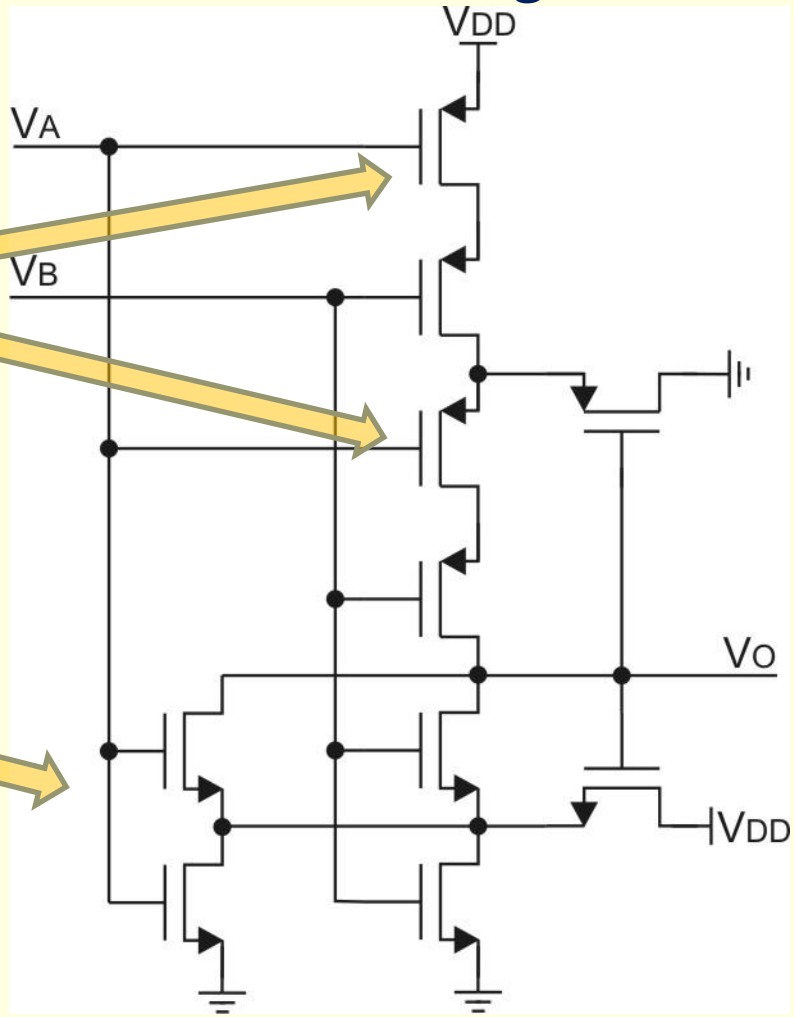


6-T Schmitt trigger - 10

NOR gate

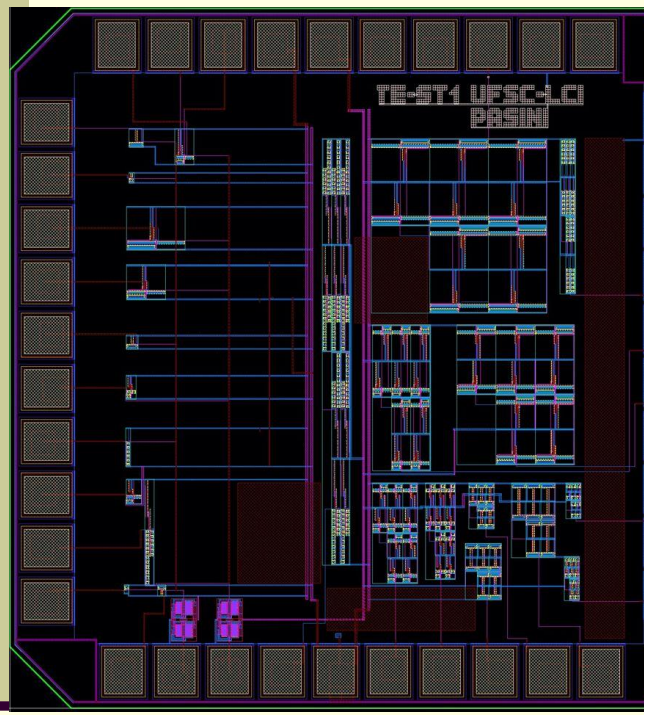


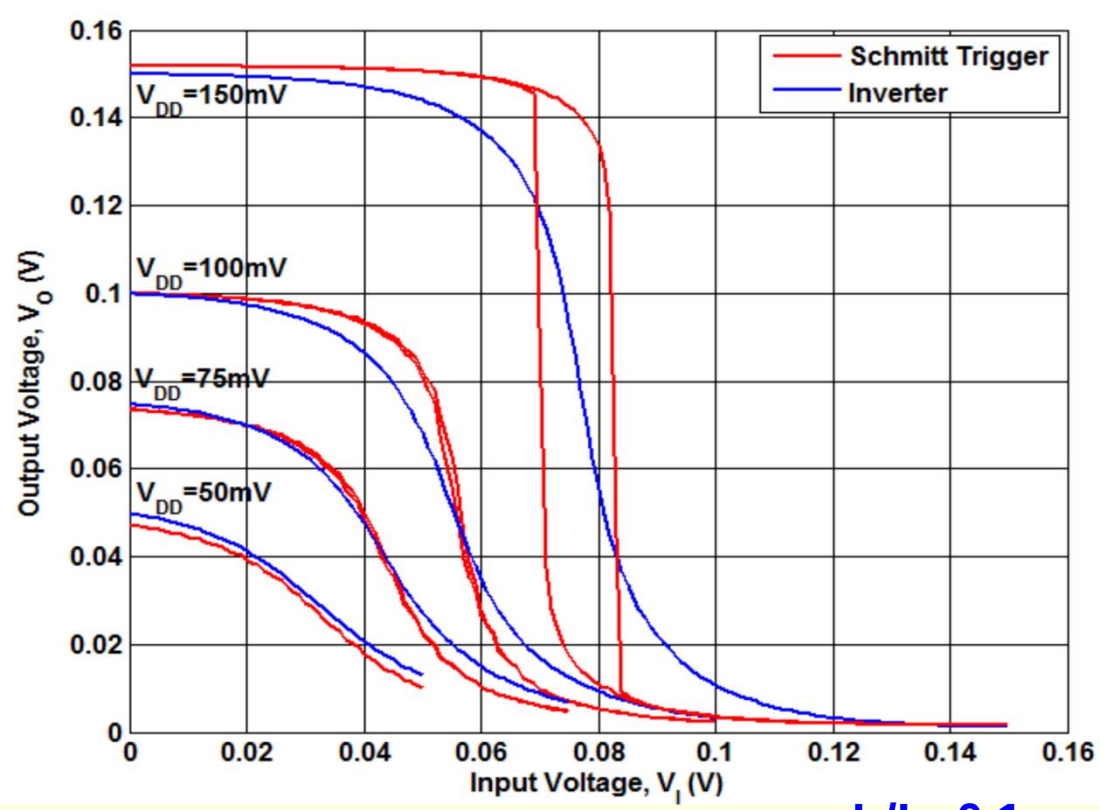
ST-NOR gate



TEST CHIP

VTC – ST x INV – V_{DD}=150, 100, 75, 50 mV





IBM 180nm
CMRF7 - MOSIS

I_1/I_0=0.1
I_2/I_0=0.4

References

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- E. Vittoz, "Weak inversion for ultimate low-power logic", in *Low-Power Electronics Design*, CRC Press, 2005.
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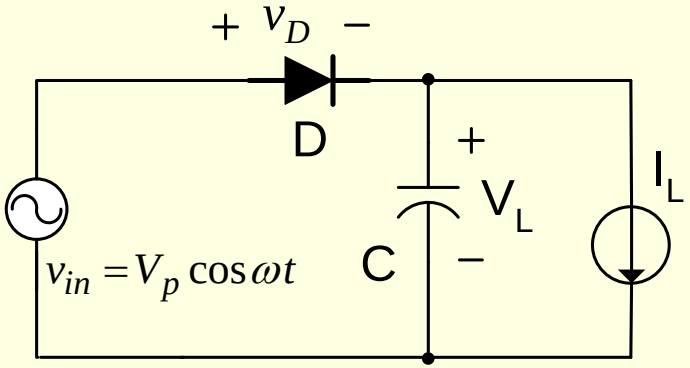
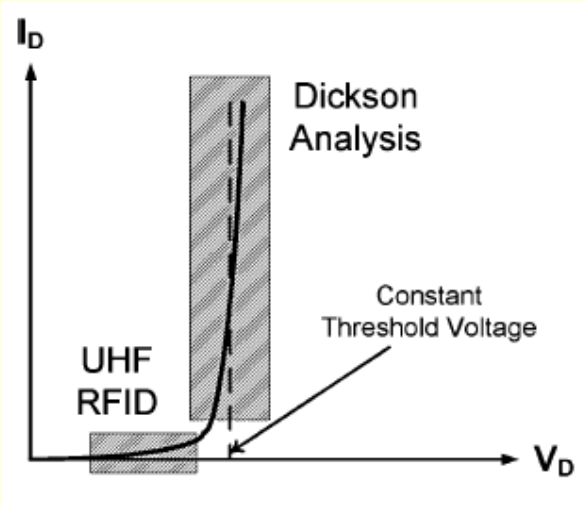
Chapter 4
ULV rectifiers

Ultra-low-voltage diode circuits

Dickson analysis of voltage multipliers: constant threshold voltage diode model, not appropriate for low voltage operation





$V_L = V_P - V_{ON}$

How to substitute the constant 'diode voltage drop' model?

Use the i-v characteristic of the diode and the load current

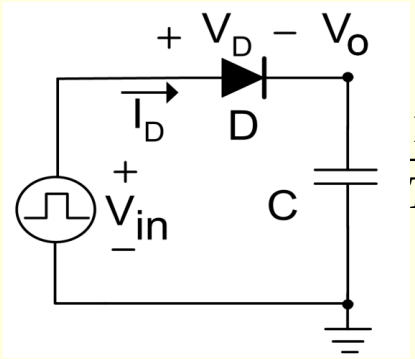
$$I_D = I_S[e^{\frac{V_D}{n\phi_t}} - 1]$$

$$\phi_t = \frac{kT}{q}$$

$n \sim 1$ to 1.5

Voltage rectifier with pure capacitive load

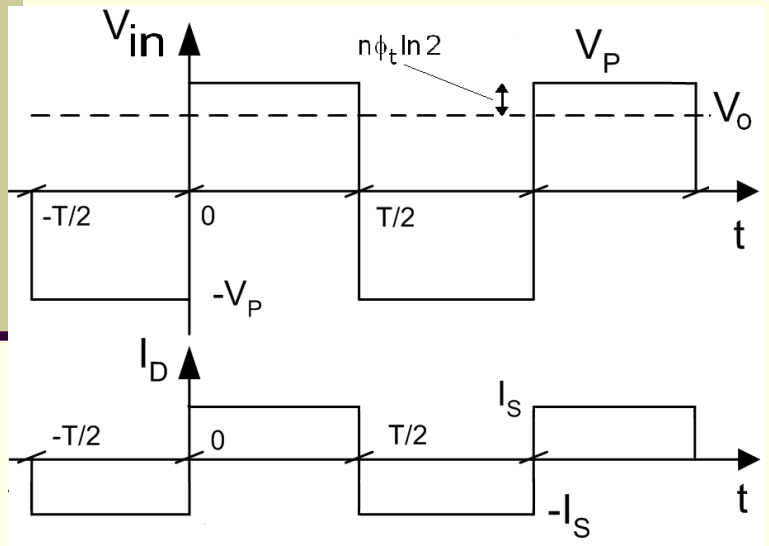
Steady-state analysis **Assumption: very low ripple (high C)**
$\rightarrow V_o \cong$ constant



$$\frac{1}{T}\int_{-T/2}^{T/2} I_D dt = \frac{I_S}{T}\int_{-T/2}^{T/2} [e^{\frac{V_D}{n\phi_t}} - 1]dt = \frac{I_S}{T}\left[\int_{-T/2}^{0}\left(e^{\left(\frac{-V_P - V_o}{n\phi_t}\right)} - 1\right)dt + \int_{0}^{T/2}\left(e^{\left(\frac{V_P - V_o}{n\phi_t}\right)} - 1\right)dt\right] = 0$$

$$\frac{V_o}{n\phi_t} = \ln\left[\frac{e^{V_P/n\phi_t} + e^{-V_P/n\phi_t}}{2}\right] = \ln\left[\cosh\left(V_P/n\phi_t\right)\right]$$

$V_P >> n\phi_t$



Power Detector

$$V_P << n\phi_t \quad \rightarrow \quad \frac{V_o}{n\phi_t} \cong \frac{1}{2}\left(\frac{V_P}{n\phi_t}\right)^2$$

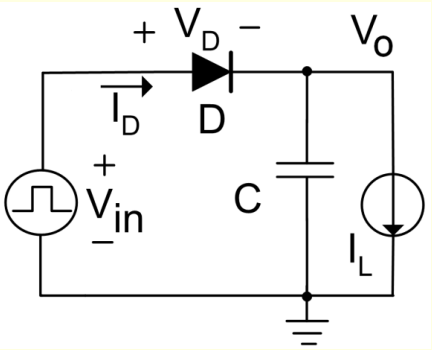
Peak Detector

Diode "ON" voltage drop

$$V_P >> n\phi_t \quad \rightarrow \quad V_L \cong V_P - n\phi_t \ln 2$$

Input

Voltage rectifier with DC load - 1



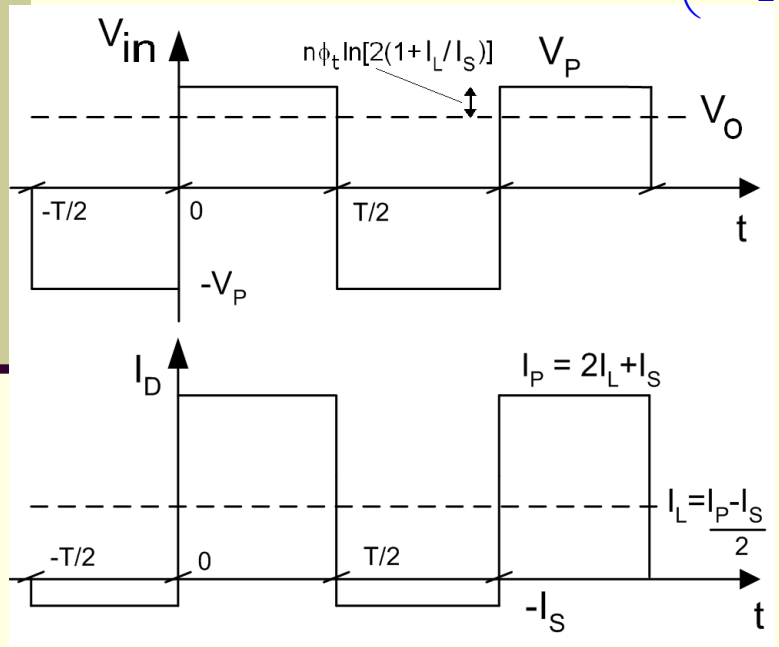
$$\frac{1}{T}\int_{-T/2}^{T/2} I_D dt = \frac{I_S}{T}\left[\int_{-T/2}^{0}\left(e^{\left(\frac{-V_P-V_o}{n\phi_t}\right)}-1\right)dt + \int_{0}^{T/2}\left(e^{\left(\frac{V_P-V_o}{n\phi_t}\right)}-1\right)dt\right] = I_L$$

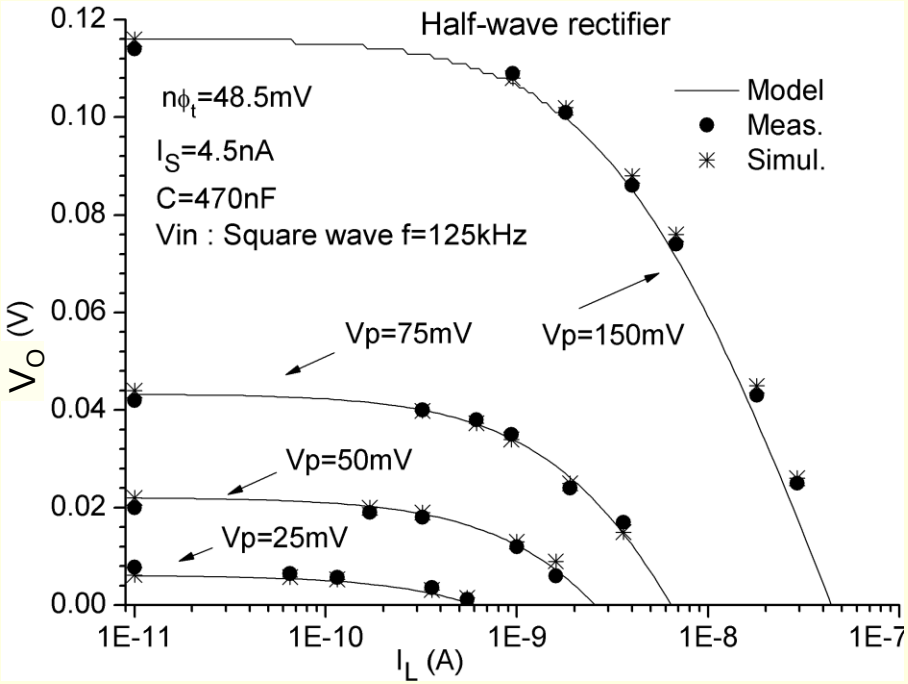
$$\frac{V_o}{n\phi_t} = \ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1+I_L/I_S}\right]$$

Diode "ON" voltage drop

Waveforms for

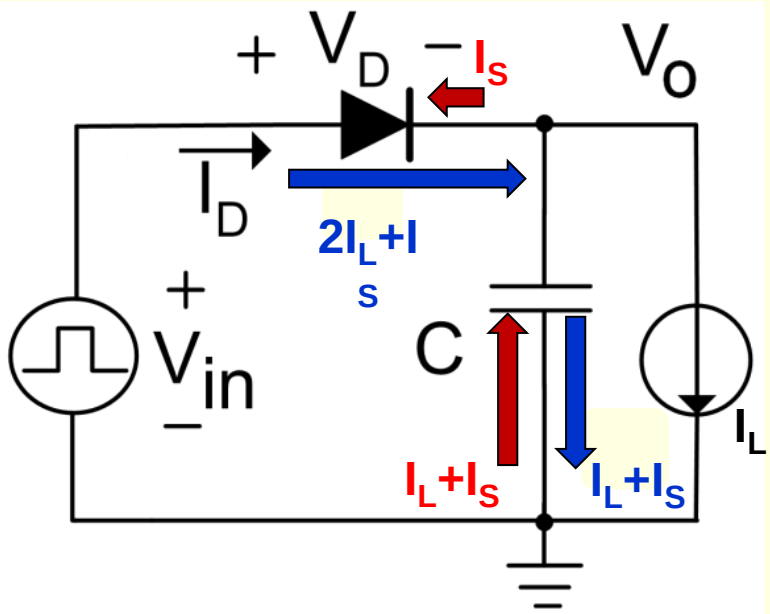
$$V_P > n\phi_t \Rightarrow V_o \cong V_P - n\phi_t \ln\left(\frac{I_P+I_S}{I_S}\right)$$

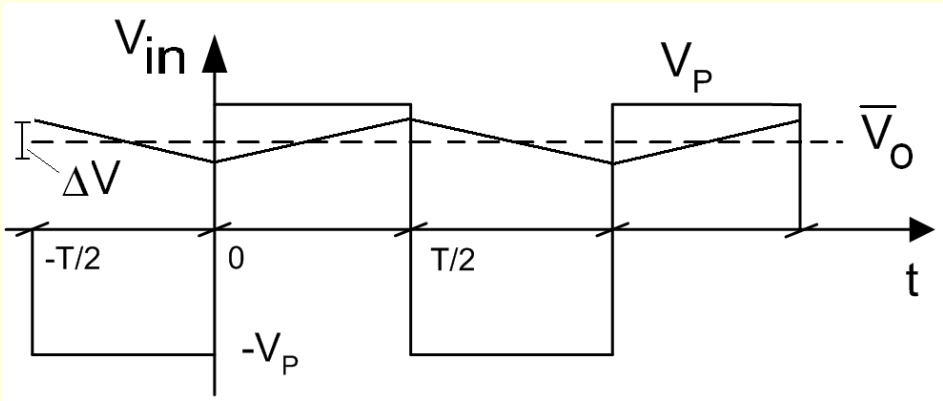




Voltage rectifier with DC load - 2

Output voltage ripple





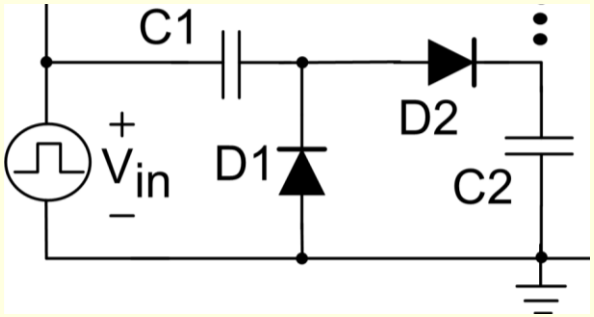
The discharge rate of the capacitor

$$I_C = \frac{dQ_C}{dt} = C\frac{dV_C}{dt} \approx I_L + I_S$$

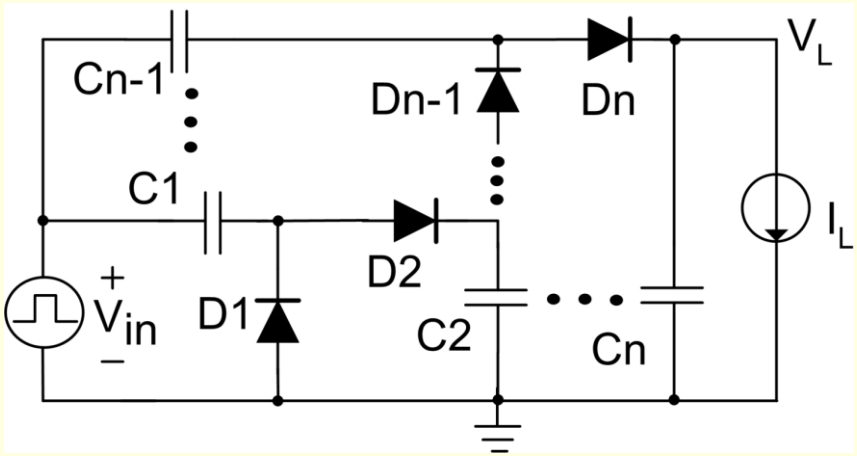
$$\int_{-T/2}^{0} dV_C = \Delta V \approx \frac{I_L + I_S}{C}\frac{T}{2} = \frac{I_L + I_S}{2fC}$$

The voltage multiplier - 1

Voltage doubler

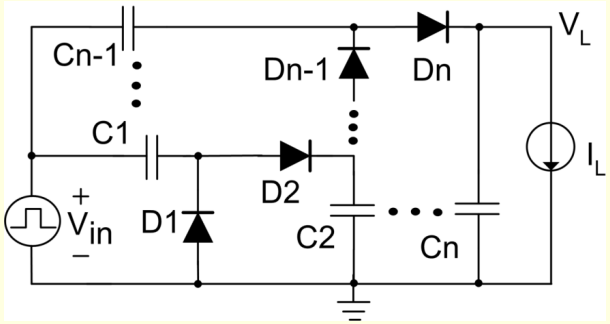


N-stage voltage multiplier



- Generation of voltages higher than V_{DD} for EEPROMs, flash memories.
- Energy harvesting for RFID tag chips

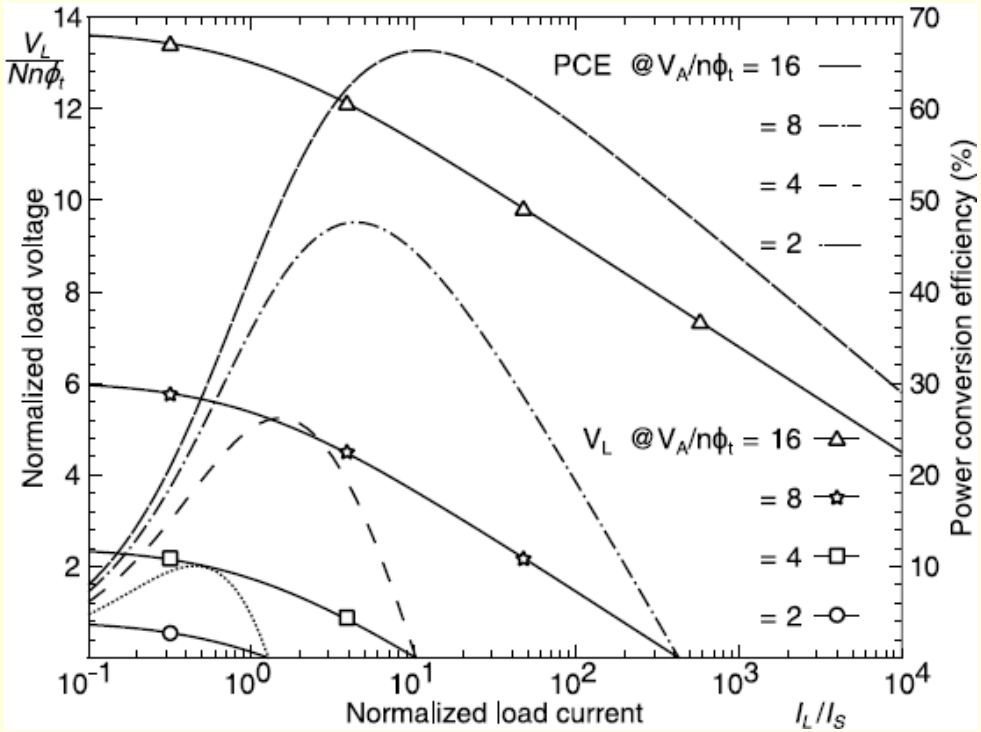
The voltage multiplier - 2



Output voltage

$$\frac{V_L}{n\phi_t} = N \ln\left[\frac{I_0(V_A/n\phi_t)}{1 + I_L/I_S}\right]$$

Modified Bessel function, first kind, order zero



Power conversion efficiency

$$PCE = \frac{P_{load}}{P_{in}} = \frac{V_L I_L}{P_{load} + P_{loss}}$$

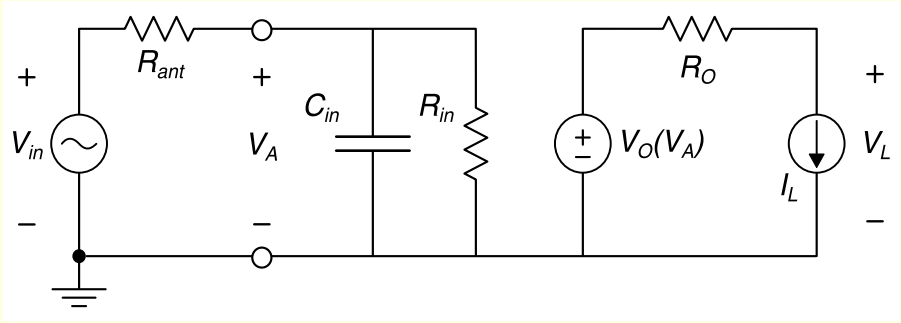
PCE is maximized for

$$\frac{I_L}{I_S} = \frac{V_L}{N n\phi_t}$$

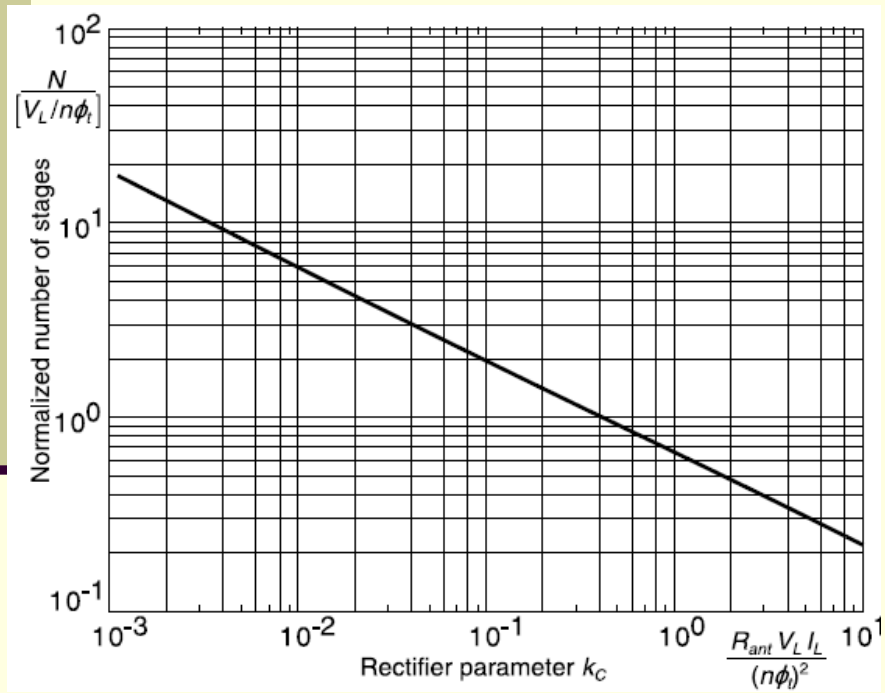
The voltage multiplier - 2

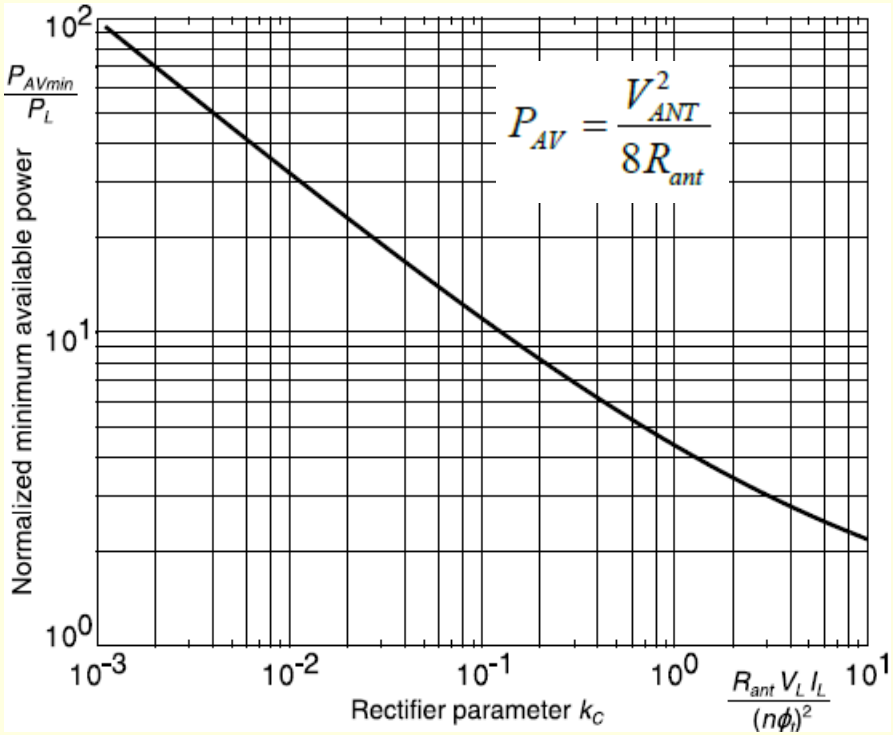
Model of the N-stage voltage multiplier

$$k_c = \frac{R_{ant} V_L I_L}{(n\phi_t)^2}$$

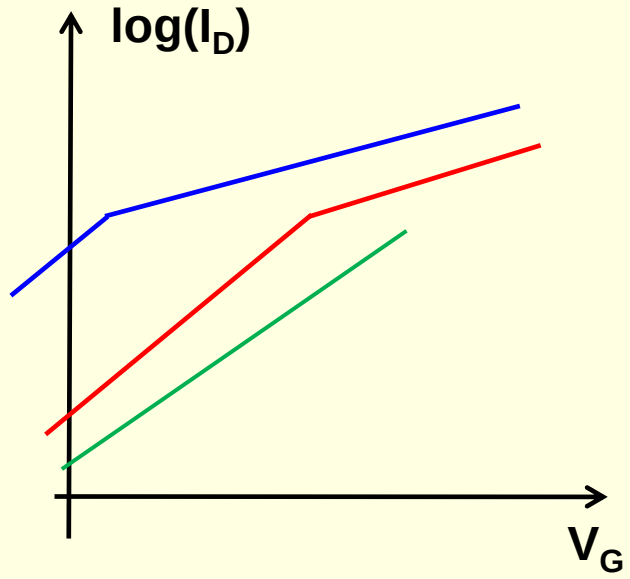


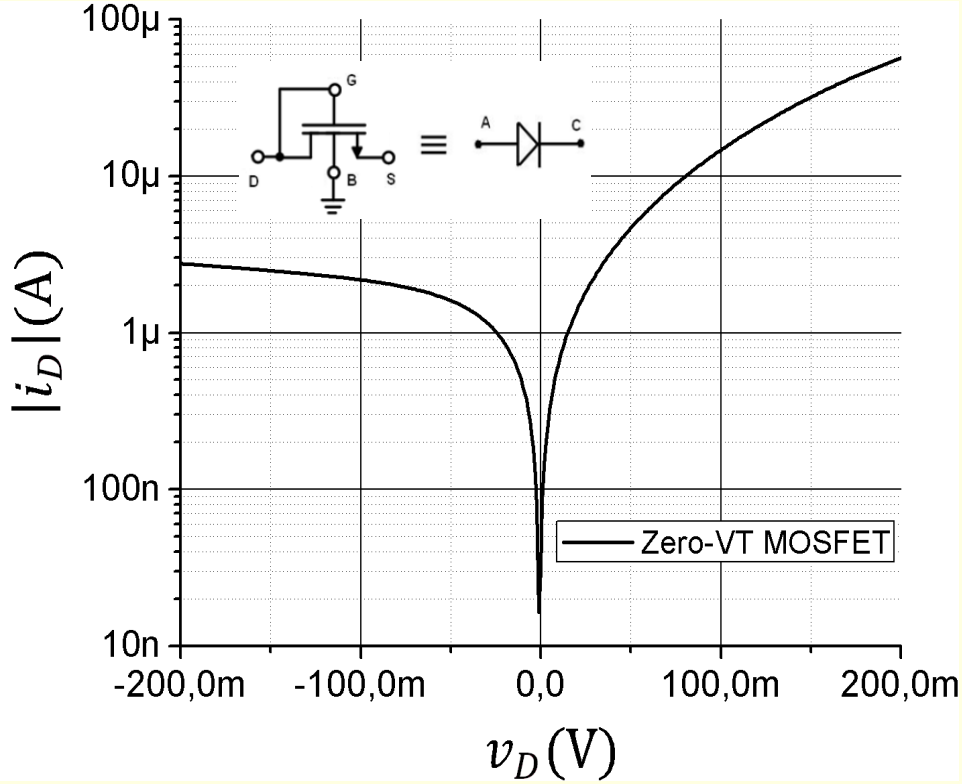
Design for minimum available power/maximum range in terms of k_c





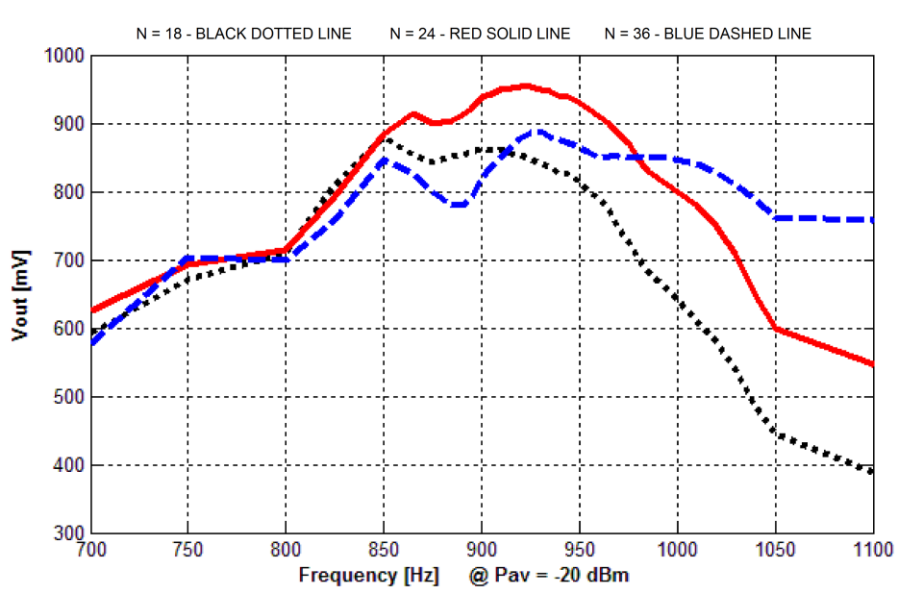
What about diodes?

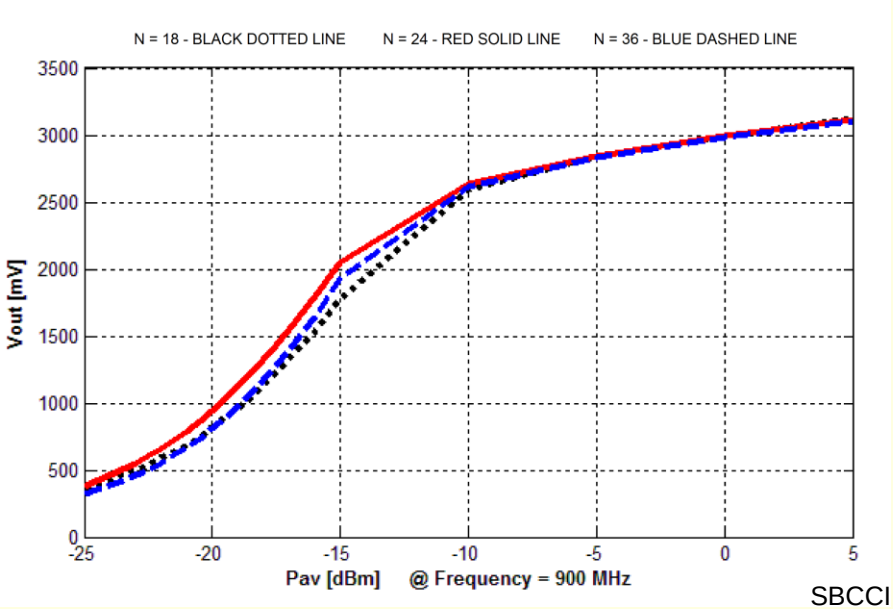




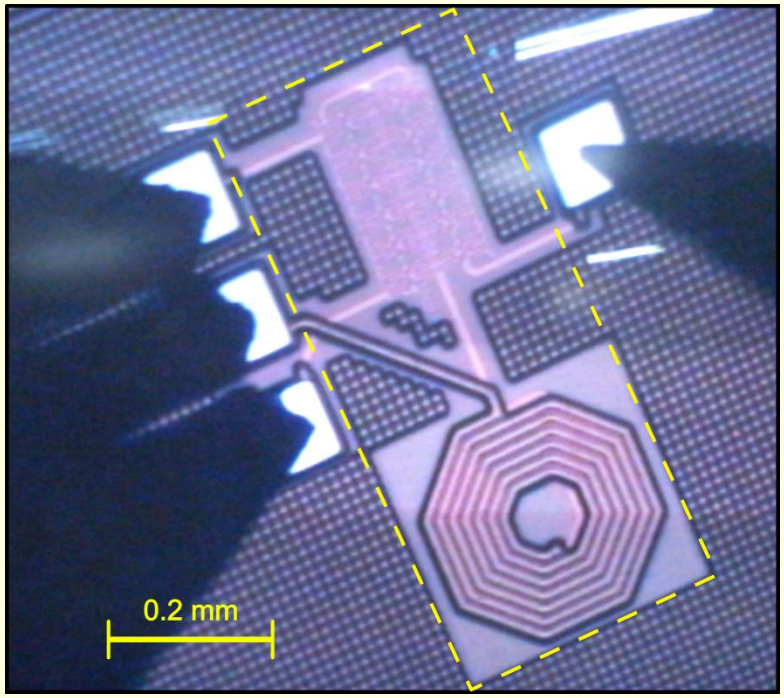
Diode-connected zero-VTMOSFET
- high drive capability

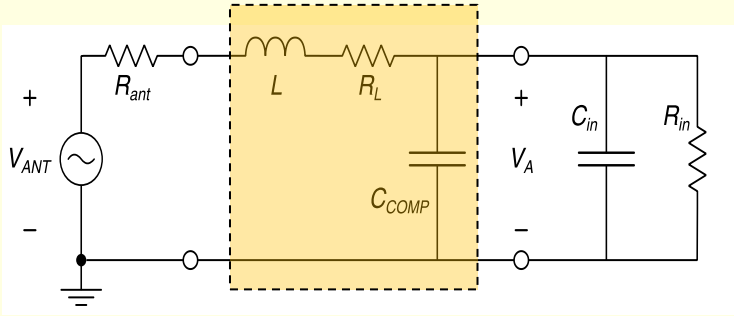
AC/DC converter in 130 nm CMOS technology





24-stage rectifier





Matching network

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- Adilson Jair Cardoso *et al.* "Teaching low voltage electronics: the case of the rectifier circuit", *IEEE International Conference on Microelectronic Systems Education (MSE),* San Diego, June 2011.
- A. J. Cardoso *et al.* , "Analysis of the rectifier circuit valid down to its low-voltage limit" , *IEEE Transactions on Circuits and Systems I: Regular Papers*, Jan. 2012.
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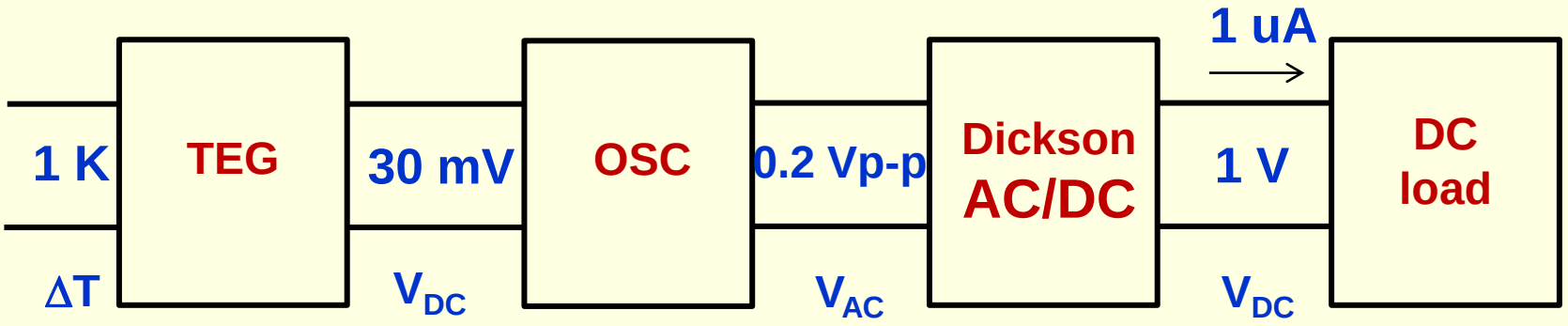
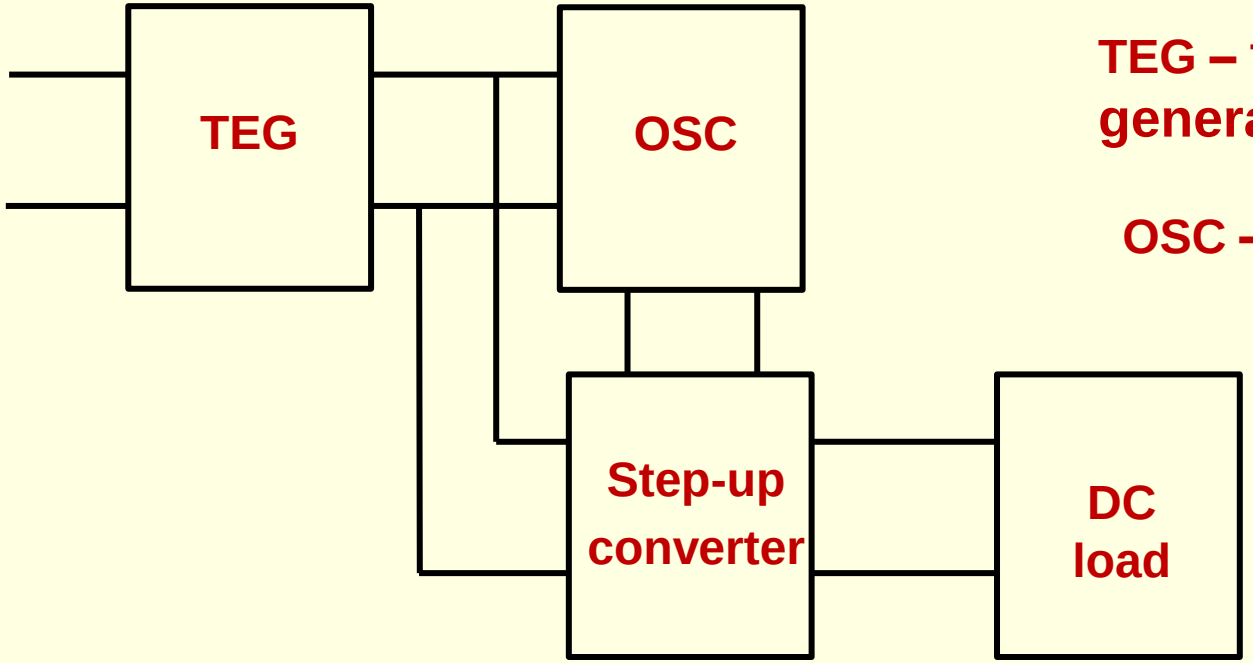
- L . G. de Carli *et al.* , “Maximizing the Power Conversion Efficiency of Ultra-Low-Voltage CMOS Multi-Stage Rectifiers,” *IEEE Transactions on Circuits and Systems I: Regular Papers,* April 2015.

Chapter 5
ULV oscillators and applications

Application of ULV oscillators for energy harvesters

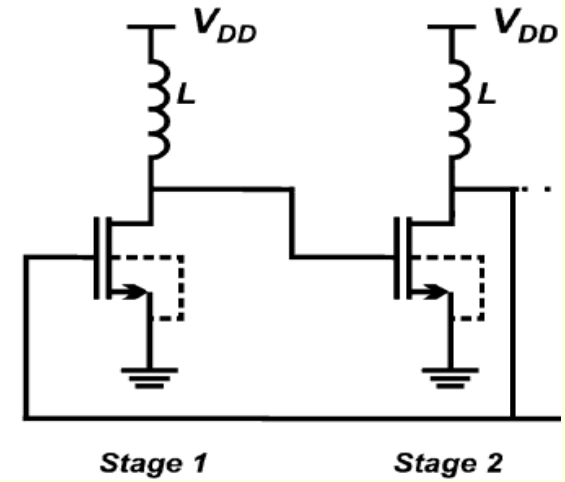




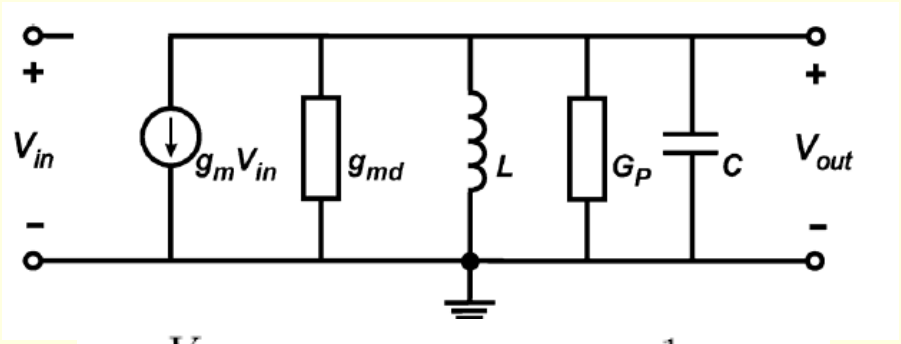
TEG – thermoelectric generator

OSC – oscillator

Inductive ring (X-coupled) oscillator - 1



Cross-coupled LC oscillator



$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{g_{md}+G_P}\frac{1}{1-j\tan\phi} \quad \text{=–1}$$

$$\tan\phi = \frac{1-LC\omega^2}{\omega L(g_{md}+G_p)}$$

Criterion for oscillation (Barkhausen)

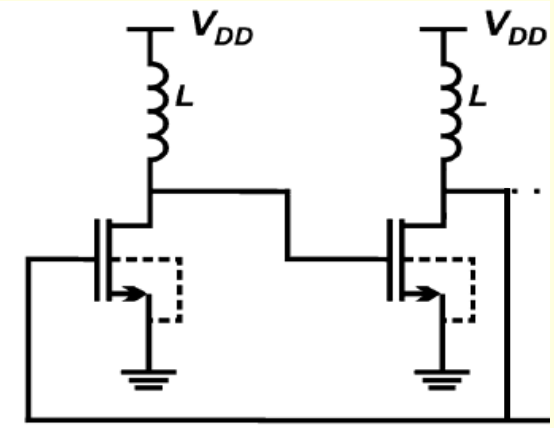
ϕ=0 & V_{out}/V_{in}=-1

$$\omega^2 LC = 1$$

$$\frac{g_m}{g_{md}+G_P} = 1$$

What´s the minimum V_{DD} for oscillation?

Inductive ring oscillator - 2



Cross-coupled LC oscillator

Oscillation frequency $\omega^2 LC = 1$

Voltage gain $\dfrac{g_m}{g_{md} + G_P} = 1$

What´s the minimum V_{DD} for oscillation?

Recall that $g_m = \dfrac{g_{ms} - g_{md}}{n}$

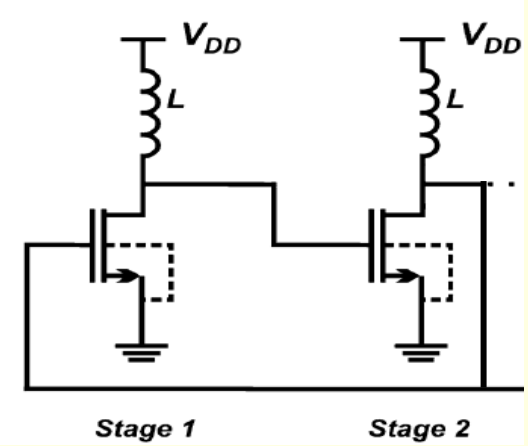
Voltage gain=1 ⇒ (i) $\dfrac{g_{ms}}{g_{md}} = 1 + n\left(1 + \dfrac{G_P}{g_{md}}\right)$

In weak inversion ⇒ (ii) $\dfrac{g_{ms}}{g_{md}} = e^{V_{DS}/\varphi_t} = e^{V_{DD}/\varphi_t}$ since $V_G = V_D = V_{DD}$

$$V_{DD,\min} = \varphi_t \ln\left[1 + n\left(1 + \frac{G_P}{g_{md}}\right)\right] = \varphi_t \ln\left[1 + n\right] \quad \text{for} \quad \frac{G_P}{g_{md}} << 1$$

Similar to the result (/2) of the CMOS inverter

Inductive ring oscillator - 3



Questions:

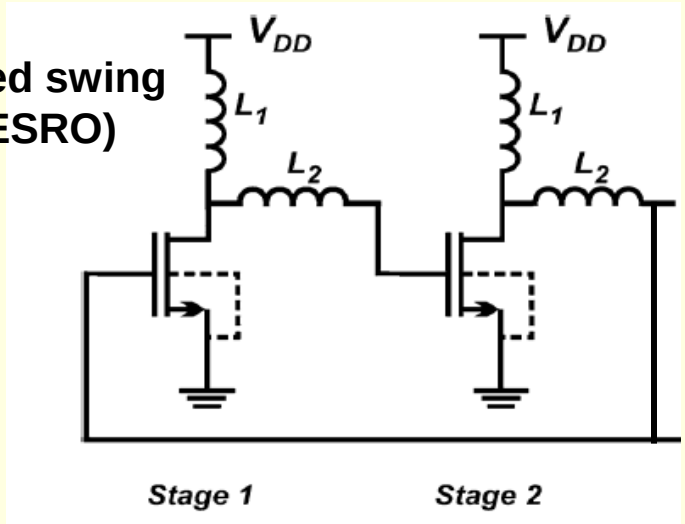
1. How to reduce $V_{DD,min}$?

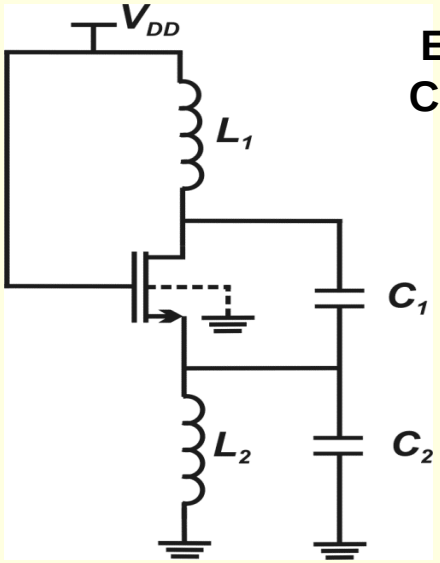
2. How to increase the V_{DD}-limited voltage swing?

Introduce voltage gain from drain to gate

Change topology, e. g., take advantage of CG gain

Enhanced swing IRO (ESRO)

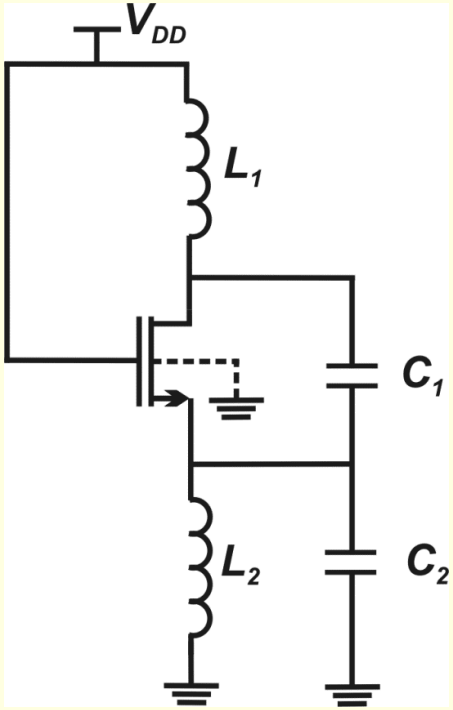


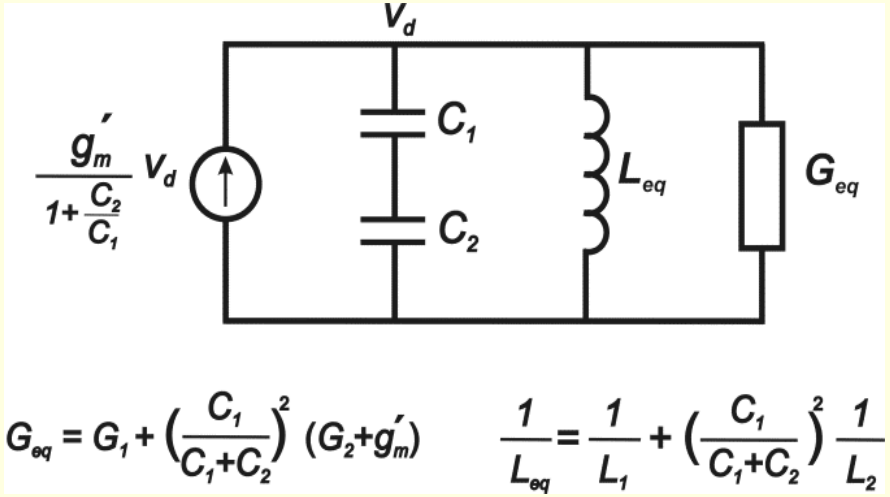


Enhanced swing Colpitts oscillator (ESCO) *

* T. W. Brown et al, *IEEE JSSC*, Aug. 2011.

The enhanced-swing Colpitts oscillator (ESCO)





$$G_{eq} = G_1 + \left(\frac{C_1}{C_1+C_2}\right)^2 (G_2+g_m') \qquad \frac{1}{L_{eq}} = \frac{1}{L_1} + \left(\frac{C_1}{C_1+C_2}\right)^2 \frac{1}{L_2}$$

$$v_s \cong \frac{v_d}{1+\frac{C_2}{C_1}} \rightarrow g_{ms}v_s - g_{md}v_d \cong g_m' v_s \qquad g_m' = g_{ms} - \left(1+\frac{C_2}{C_1}\right) g_{md}$$

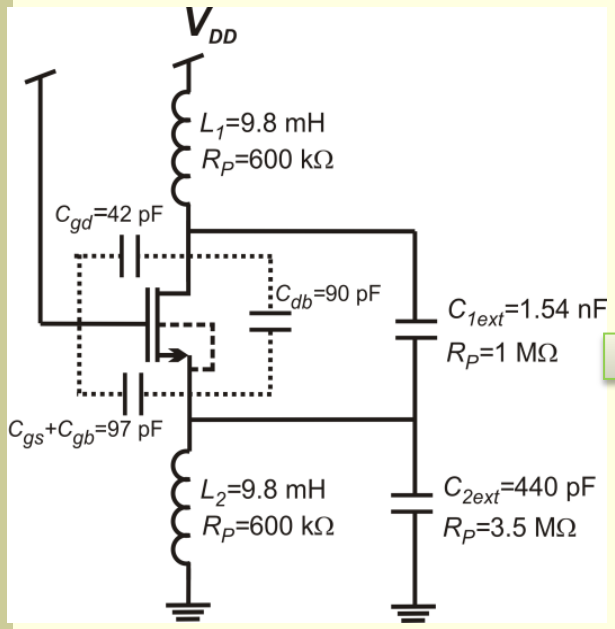
For lossless inductors and capacitors

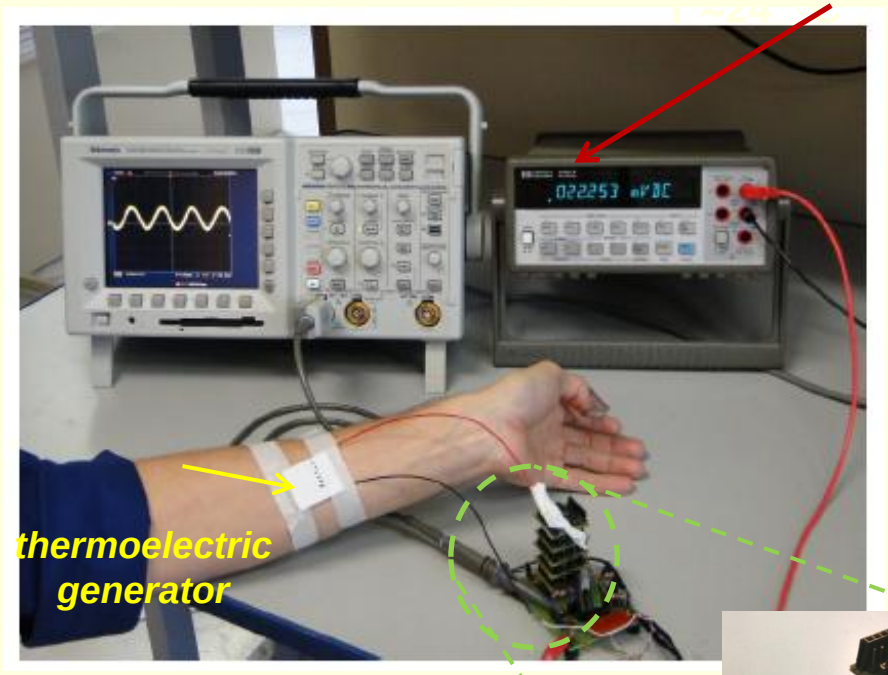
Weak inversion

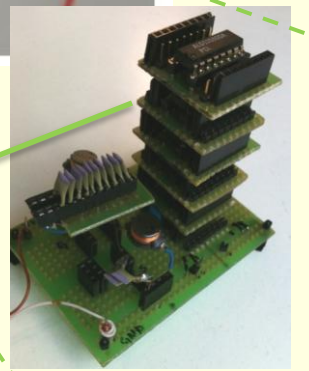
$$V_{DD\lim} = \frac{kT}{q} \ln\left(1+\frac{C_2}{C_1}\right)$$

Colpitts oscillator: first prototype

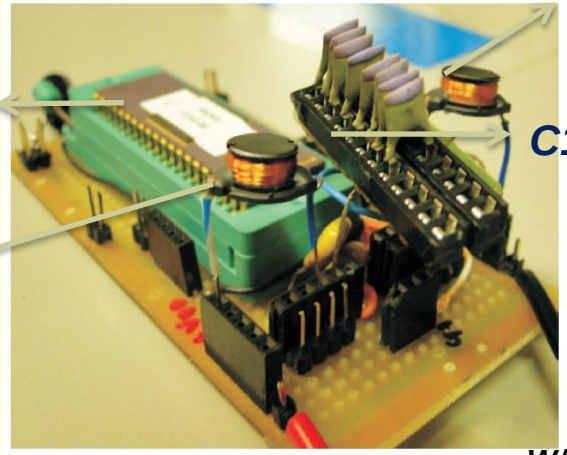
Off-the-shelf components





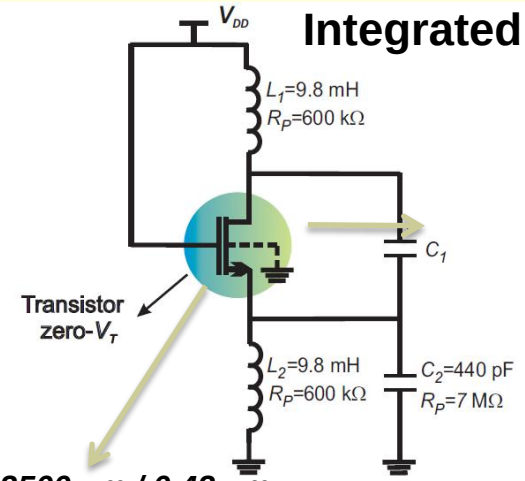


Colpitts oscillator: second prototype

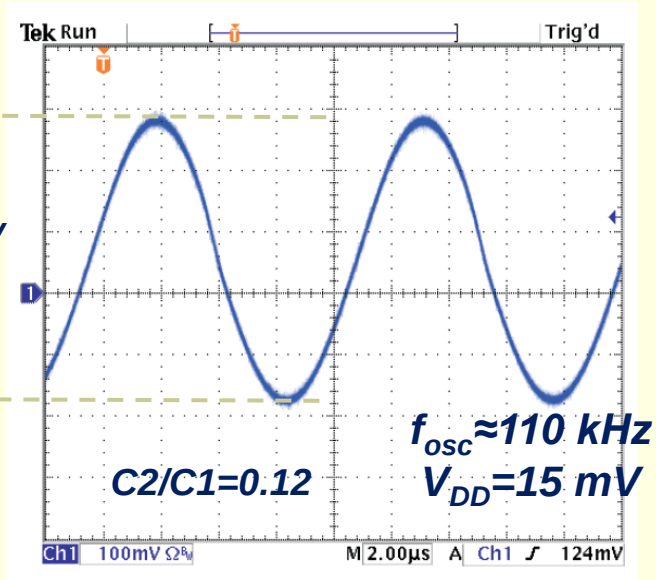


Zero-VT
IBM 130 nm

Integrated Zero-VT MOSFET



W/L = 2500 µm / 0.42 µm



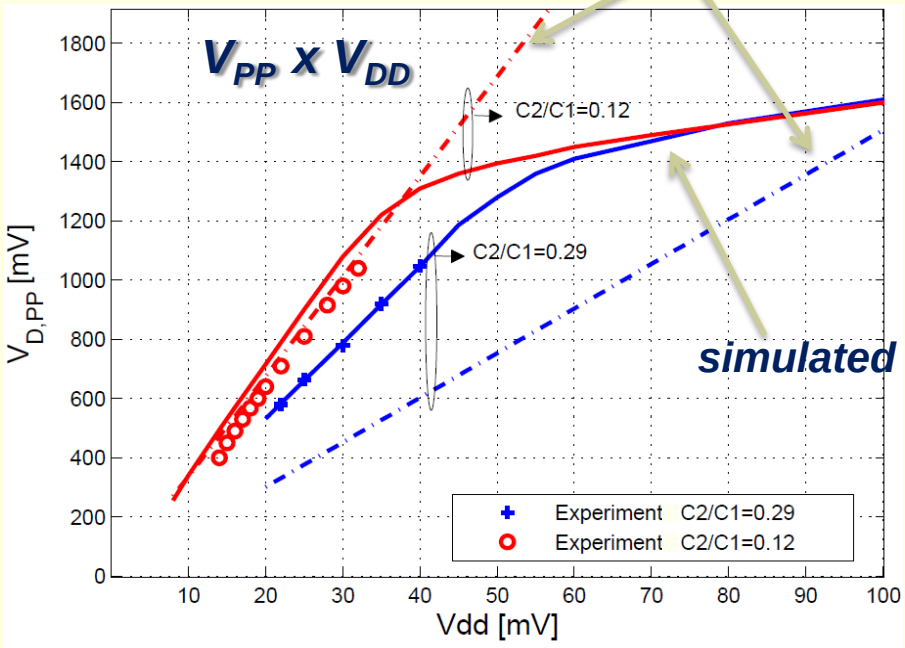
V_{PP}≈440 mV

f_{osc}≈110 kHz

V_{DD}=15 mV

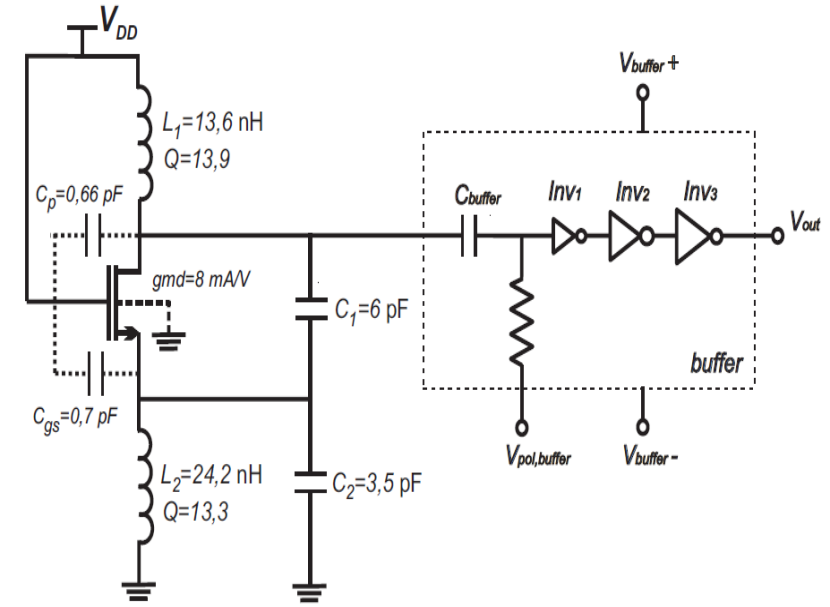
C2/C1=0.12

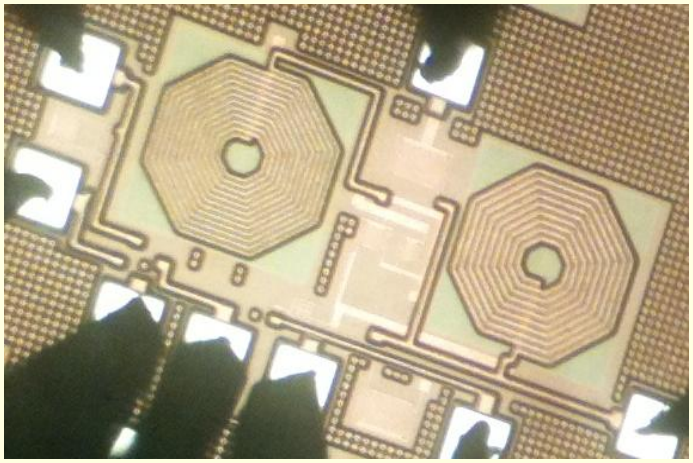
calculated



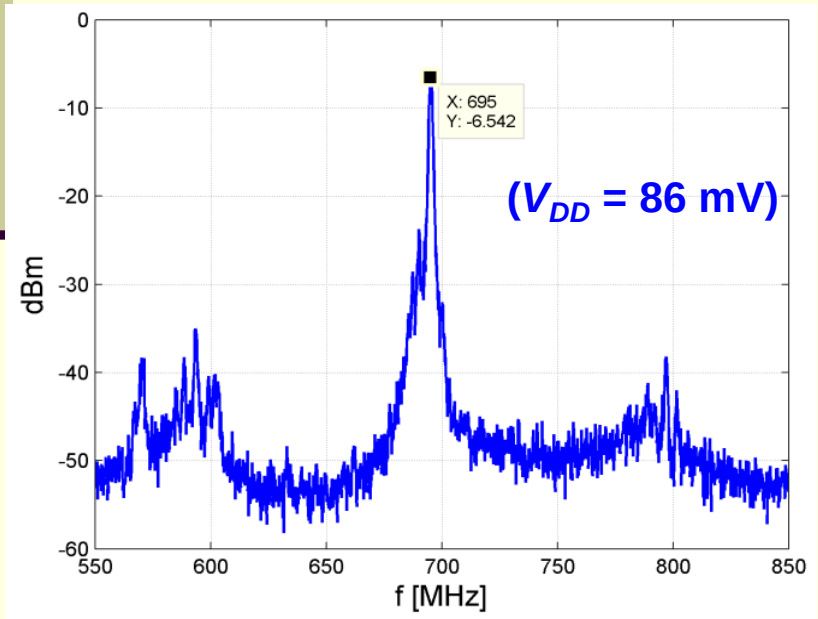
simulated

Colpitts oscillator – IC prototype

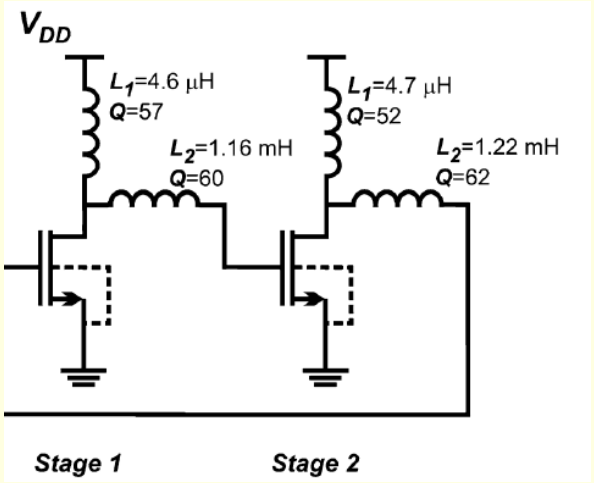




130 nm technology



Enhanced-swing ring oscillator (ESRO)



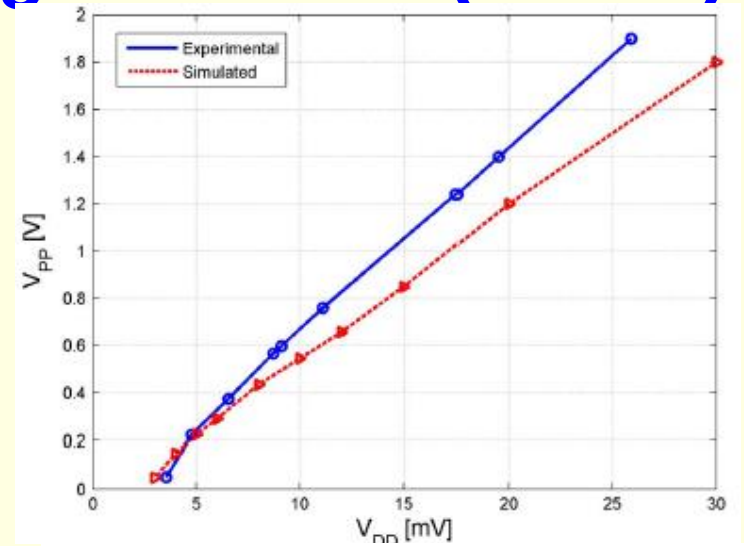
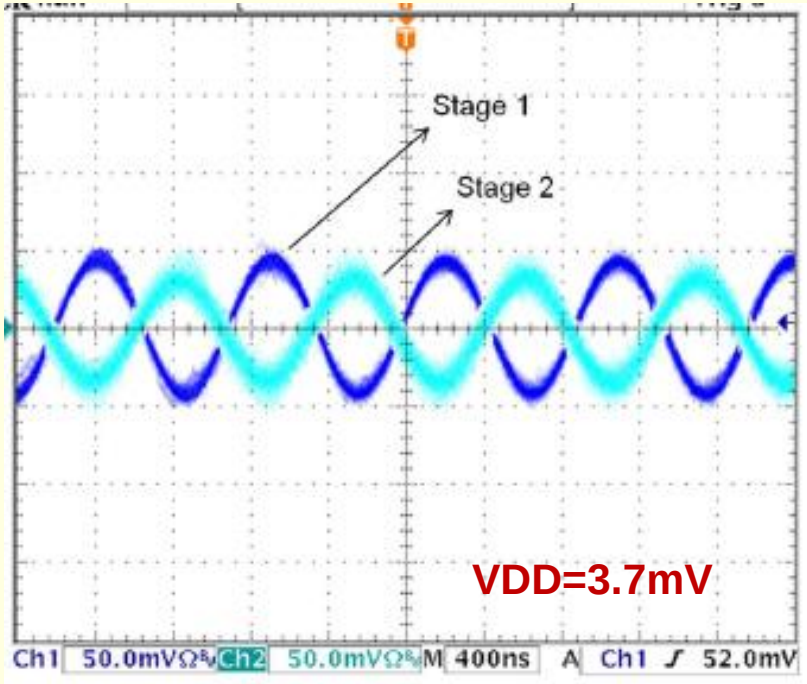


Fig. 12. Simulated (dotted line) and experimental (solid line) peak-to-peak gate voltage versus supply voltage of the ES inductive-load ring oscillator.



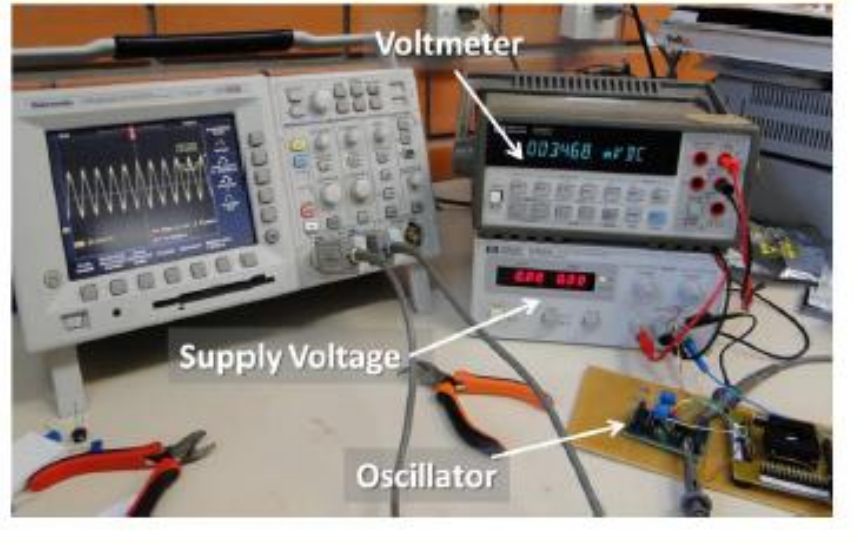


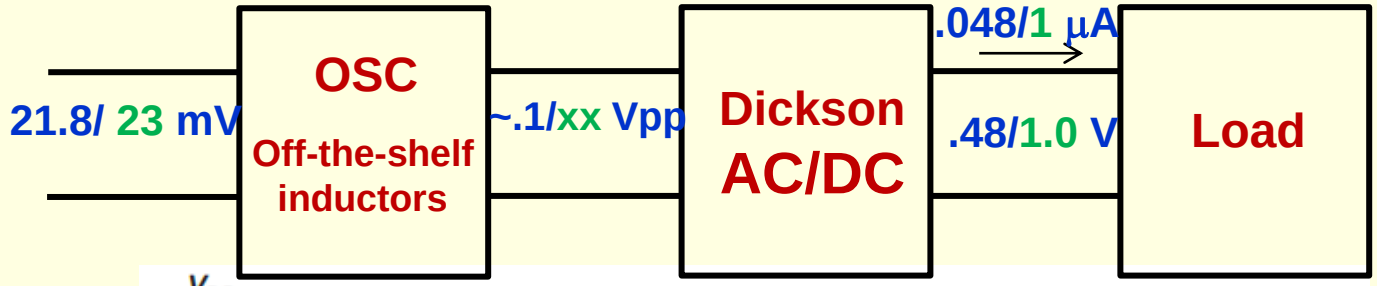
TABLE I
EXPERIMENTAL RESULTS FOR THE OSCILLATION FREQUENCY AND MINIMUM SUPPLY VOLTAGE OF THE OSCILLATOR TOPOLOGIES

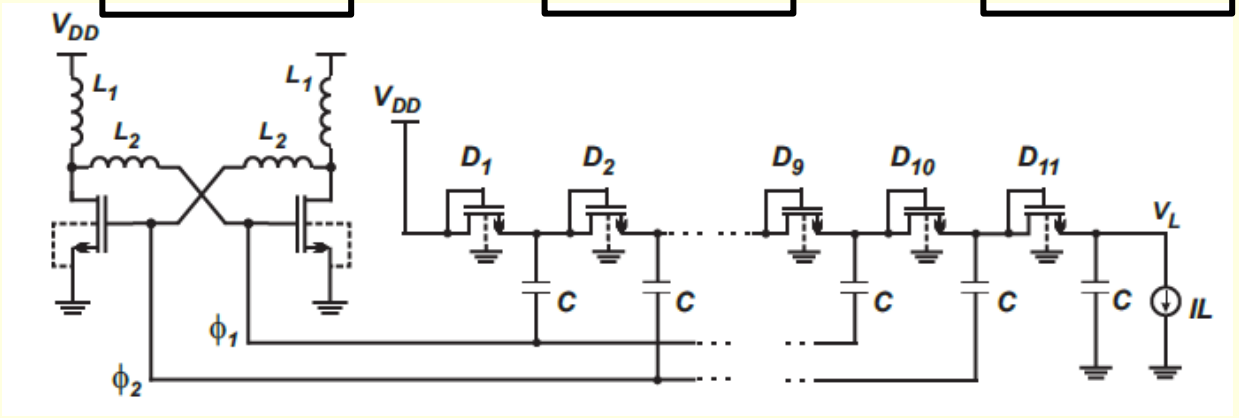
Topology	Theoretical V_{dd} (min) *	IC prototype 130nm CMOS		Discrete prototype	
		V_{dd} (min)	f_{osc}	V_{dd} (min)	f_{osc}
ILRO	$\phi_t \ln(1+n)$	53 mV	550 MHz	50 mV	11 MHz
ESRO	$\phi_t \ln\left(1+n\frac{L_1}{L_1+L_2}\right)$	32 mV	400 MHz	3.5 mV	1.1 MHz
ESCO	$\phi_t \ln\left(1+\frac{C_2/C_1}{1+L_1/L_2}\right)$	86 mV	700 MHz	15 mV	108 kHz

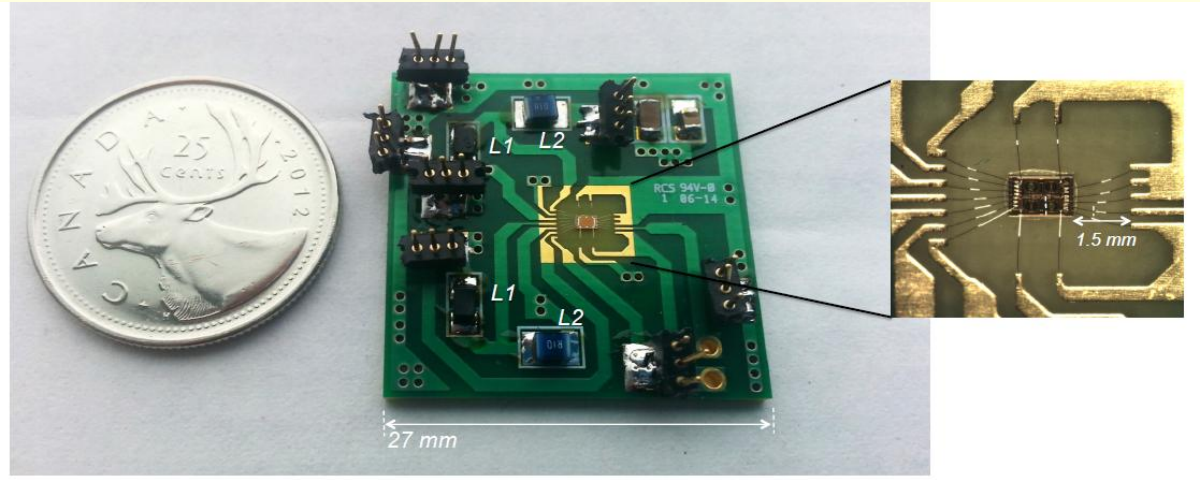
* For lossless passive devices and operation of MOSFETs in weak inversion

Values of components:
ILRO – IC prototype – L = 100 nH, Q = 8.
ILRO – discrete prototype – L = 4.6 uH, Q = 50.
ESRO – IC prototype – L_1 = 20 nH, Q_1 = 9; L_1 = 80 nH, Q_2 = 8.
ESRO – discrete prototype – L_1 = 4.6 uH, Q_1 = 55, L_2 = 1.2 mH, Q_2 = 60.
ESCO – IC prototype – L_1 = 13.6 nH, Q_1 = 13.9, L_2 = 24.2 nH, Q_2 = 13.3, C_1 = 6 pF, C_2 = 3.5 pF.
ESCO – discrete prototype – L_1 = L_2 = 9.8 mH, Q_1 = Q_2 = 80, C_1 = 1.54 nF, C_2 = 0.44 nF.

Energy harvester







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- C. Galup-Montoro, M. C. Schneider, and M. B. Machado, “Ultra-low-voltage operation of CMOS analog circuits: amplifiers, oscillators, and rectifiers,” *IEEE Trans. on Circuits and Syst. II*, *Exp. Briefs*, Dec. 2012.
- M. B. Machado *et al.* , “On the minimum supply voltage for MOSFET oscillators”, *IEEE Transactions on Circuits and Systems I: Regular Papers*, Feb 2014.
- M. B. Machado *et al.*,"Fully integrated inductive ring oscillators operating at VDD below 2kT/q,", *Analog Integrated Circuits and Signal Processing*, Jan 2015.